XC2064/XC2018 Logic Cell™ Array

Product Specification

FEATURES

- Fully Field-Programmable:
  - I/O functions
  - Digital logic functions
  - Interconnections
- General-purpose array architecture
- Complete user control of design cycle
- Compatible arrays with logic cell complexity equivalent to 1200 and 1800 gates
- Standard product availability
- 100% factory-tested
- Selectable configuration modes
- Low-power, CMOS, static-memory technology
- Performance equivalent to TTL SSI/MSI
- TTL or CMOS input thresholds
- Complete development system support
  - XACT Design Editor
  - Schematic Entry
  - XACTOR In-Circuit Emulator
  - Macro Library
  - Timing Calculator
  - Logic and Timing Simulator
  - Auto Place / Route

DESCRIPTION

The Logic Cell™ Array (LCA™) is a high density CMOS integrated circuit. Its user-programmable array architecture is made up of three types of configurable elements: Input/Output Blocks, logic blocks and Interconnect. The designer can define individual I/O blocks for interface to external circuitry, define logic blocks to implement logic functions and define interconnection networks to compose larger scale logic functions. The XACT™ Development System provides interactive graphic design capture and automatic routing. Both logic simulation and in-circuit emulation are available for design verification.

The Logic Cell Array is available in a variety of logic capacities, package styles, temperature ranges and speed grades.

Part Number	Logic Capacity (gates)	Configurable Logic Blocks	User I/Os	Configuration Program (bits)
XC2064	1200	64	58	12038
XC2018	1800	100	74	17878

The LCA logic functions and interconnections are determined by data stored in internal static-memory cells. On-chip logic provides for automatic loading of configuration data at power-up. The program data can reside in an EEPROM, EPROM or ROM on the circuit board or on a floppy disk or hard disk. The program can be loaded in a number of modes to accommodate various system requirements.

ARCHITECTURE

The general structure of a Logic Cell Array is shown in Figure 1. The elements of the array include three categories of user programmable elements: I/O Blocks (IOBs), Configurable Logic Blocks (CLBs) and Programmable Interconnections. The I/OBs provide an interface between the logic array and the device package pins. The CLBs perform user-specified logic functions, and the interconnect resources are programmed to form networks that carry logic signals among the blocks.

LCA configuration is established through a distributed array of memory cells.The XACT development system generates the program used to configure the Logic Cell Array which includes logic to implement automatic configuration.

Configuration Memory

The configuration of the Logic Cell Array is established by programming memory cells which determine the logic functions and interconnections. The memory loading process is independent of the user logic functions.

The static memory cell used for the configuration memory in the Logic Cell Array has been designed specifically for high reliability and noise immunity. Based on this design, which has been patented, integrity of the LCA configuration memory is assured even under adverse conditions. Compared with other programming alternatives, static memory provides the best combination of high density, high performance, high reliability and comprehensive testability. As shown in Figure 2, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing data to the cell. The cell is only written during configuration and only read during readback. During normal operation the pass transistor is "off" and does not affect the stability of the cell. This is quite different from the normal operation of conventional memory devices, in which the cells are continuously read and rewritten.

The outputs Q and $\overline{Q}$ control pass-transistor gates directly. The absence of sense amplifiers and the output capacitive load provide additional stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. In reliability testing no soft errors have been observed, even in the presence of very high doses of alpha radiation.

Input/Output Block

Each user-configurable I/O block (IOB) provides an interface between the external package pin of the device and the internal logic. Each I/O block includes a programmable input path and a programmable output buffer. It also provides input clamping diodes to provide protection from electro-static damage, and circuits to protect the LCA from latch-up due to input currents. Figure 3 shows the general structure of the I/O block.

The input buffer portion of each I/O block provides threshold detection to translate external signals applied to the package pin to internal logic levels. The input buffer threshold of the I/O blocks can be programmed to be compatible with either TTL (1.4 V) or CMOS (2.2 V) levels.

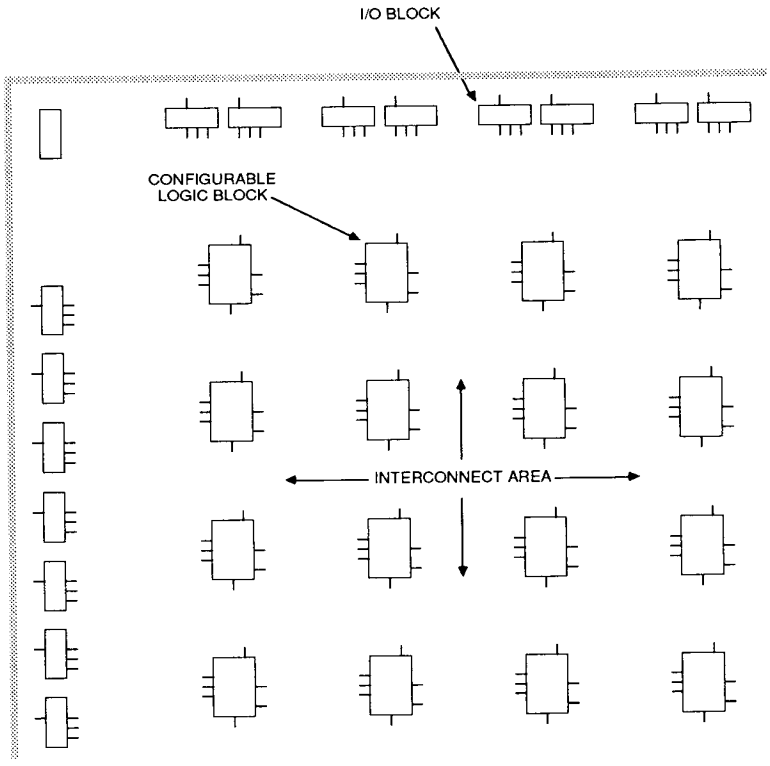

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Figure 1. Logic Cell Array Structure

The buffered input signal drives both the data input of an edge-triggered D flip-flop and one input of a two-input multiplexer. The output of the flip-flop provides the other input to the multiplexer. The user can select either the direct input path or the registered input, based on the content of the memory cell controlling the multiplexer. The I/O Blocks along each edge of the die share common clocks. The flip-flops are reset during configuration as well as by the active-low chip $\overline{\text{RESET}}$ input.

Output buffers in the I/O blocks provide 4-mA drive for high fan-out CMOS or TTL-compatible signal levels. The output data (driving I/O block pin O) is the data source for the I/O block output buffer. Each I/O block output buffer is controlled by the contents of two configuration memory cells which turn the buffer ON or OFF or select 3-state buffer control. The user may also select the output buffer 3-state control (I/O block pin TS). When this I/O block output control signal is High (a logic "1"), the buffer is disabled and the package pin is high-impedance.

Configurable Logic Block

An array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix in the

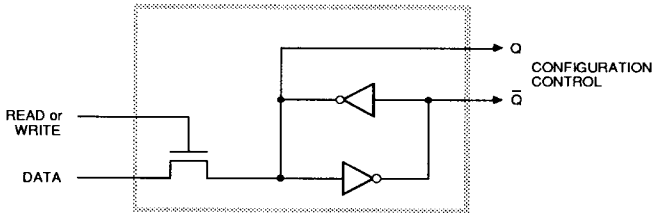


Figure 2. Configuration Memory Cell

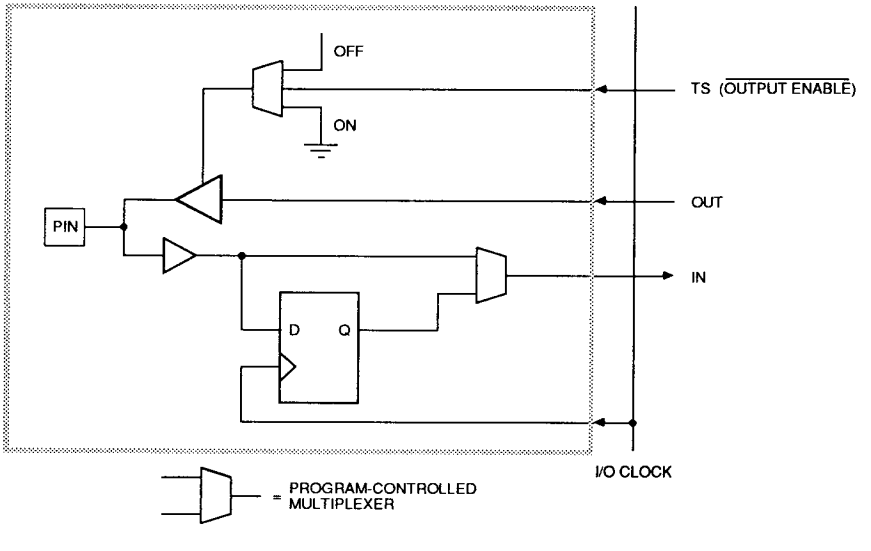


Figure 3. I/O Block

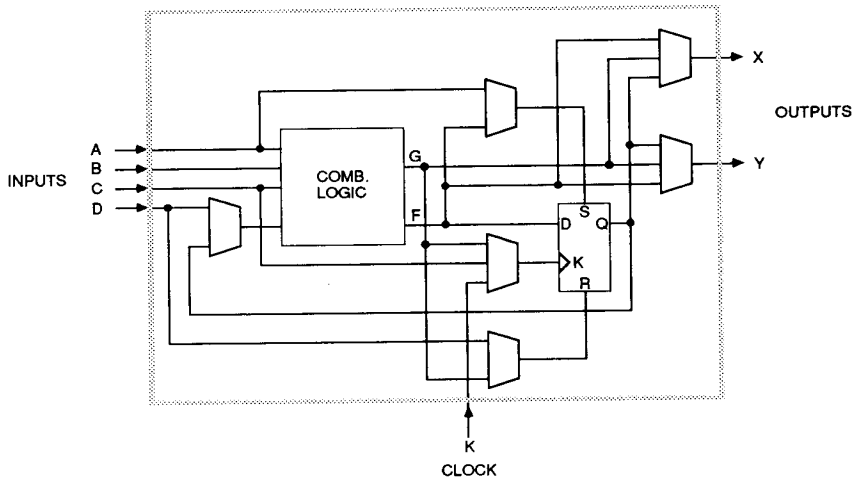


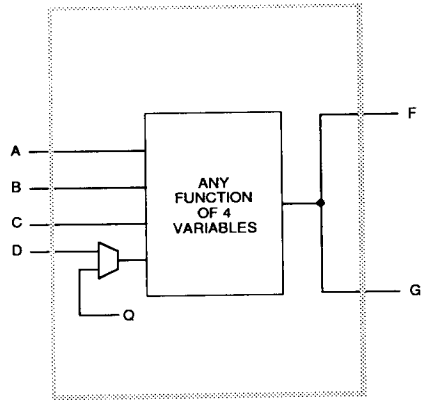
Figure 4. Configurable Logic Block

center of the device. The XC2064 has 64 such blocks arranged in an 8-row by 8-column matrix. The XC2018 has 100 logic blocks arranged in a 10 by 10 matrix.

Each logic block has a combinatorial logic section, a storage element, and an internal routing and control section. Each CLB has four general-purpose inputs: A, B, C and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks. Figure 4 shows the resources of a Configurable Logic Block.

The logic block combinatorial logic uses a table look-up memory to implement Boolean functions. This tech-nique can generate any logic function of up to four variables with a high speed sixteen-bit memory. The propagation delay through the combinatorial network is independent of the function generated. Each block can perform any function of four variables or any two functions of three variables each. The variables may be selected from among the four inputs and the block's storage element output "Q". Figure 5 shows various options which may be specified for the combinatorial logic.

If the single 4-variable configuration is selected (Option 1), the F and G outputs are identical. If the 2-function alternative is selected (Option 2), logic functions F and G may be independent functions of three variables each. The three variables can be selected from among the four logic block inputs and the storage element output "Q". A third form of the combinatorial logic (Option 3) is a special case of the 2-function form in which the B input dynamically selects between the two function tables providing a single



OPTION 1

1 FUNCTION OF 4 VARIABLES

merged logic function output. This dynamic selection allows some 5-variable functions to be generated from the four block inputs and storage element Q. Combinatorial functions are restricted in that one may not use both its storage element output Q and the input variable of the logic block pin "D" in the same function.

If used, the storage element in each Configurable Logic Block (Figure 6) can be programmed to be either an edge-sensitive "D" type flip-flop or a level-sensitive "D" latch. The clock or enable for each storage element can be selected from:

- The special-purpose clock input K
- The general-purpose input C
- The combinatorial function G

The user may also select the clock active sense within each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device.

The storage element data input is supplied from the function F output of the combinatorial logic. Asynchronous SET and RESET controls are provided for each storage element. The user may enable these controls independently and select their source. They are active

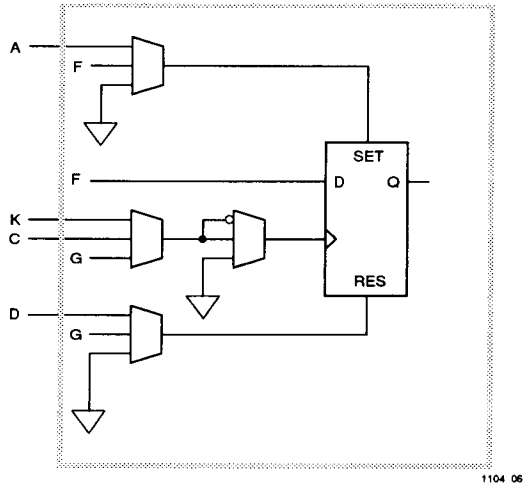


Figure 6. CLB Storage Elememt

High inputs and the asynchronous reset is dominant. The storage elements are reset by the active-Low chip $\overline{\text{RESET}}$ pin as well as by the initialization phase preceding configuration. If the storage element is not used, it is disabled.

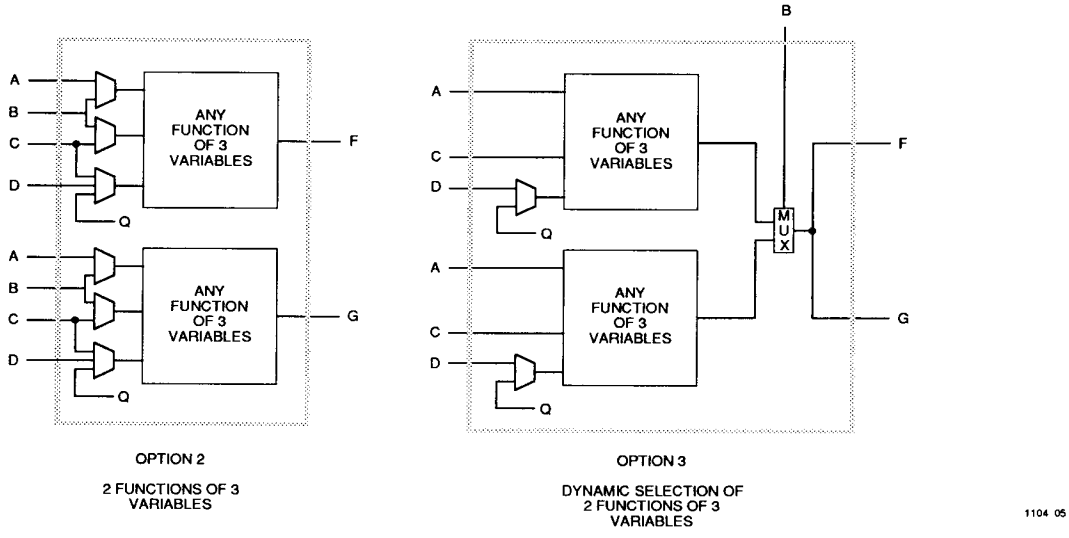


Figure 5. CLB Combinatorial Logic Options
Note: Variables D and Q can not be used in the same function.

The two block outputs, X and Y, can be driven by either the combinatorial functions, F or G, or the storage element output Q (Figure 4). Selection of the outputs is completely interchangeable and may be made to optimize routing efficiencies of the networks interconnecting the logic blocks and I/O blocks.

PROGRAMMABLE INTERCONNECT

Programmable interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into desired networks. All interconnections are composed of metal segments, with programmable switching points provided to implement the necessary routing. Three types of resources accommodate different types of networks:

- General purpose interconnect
- Long lines
- Direct connection

General-Purpose Interconnect

General-purpose interconnect, as shown in Figure 7a, is composed of four horizontal metal segments between the rows and five vertical metal segments between the columns of logic and I/O blocks. Each segment is only the "height" or "width" of a logic block. Where these segments would cross at the intersections of rows and columns, switching matrices are provided to allow interconnections of metal segments from the adjoining rows and columns. Switches in the switch matrices and on block outputs are specially designed transistors, each controlled by a configuration bit.

Logic-block output switches provide contacts to adjacent general interconnect segments and therefore to the switching matrix at each end of those segments. A switch matrix can connect an interconnect segment to other segments to form a network. Figure 7a shows the general interconnect used to route a signal from one logic block to three other logic blocks. As shown, combinations of closed switches in a switch matrix allow multiple branches for each network. The inputs of the logic or I/O blocks are multiplexers that can be program-med with configuration bits to select an input network from the adjacent interconnect segments. Since the switch connections to block inputs are unidirectional (as are block outputs) they are usable *only* for input connection. The development system software provides automatic routing of these interconnections. Interactive routing is also available for design optimization. This is accomplished by selecting a network and then toggling the states of the interconnect points by selecting them with the "mouse". In this mode, the connections through the switch matrix may be established by selecting pairs of matrix pins. The switching matrix combinations are indicated in Figure 7b.

Special buffers within the interconnect area provide periodic signal isolation and restoration for higher general interconnect fan-out and better performance. The repowering buffers are bidirectional, since signals must be able to propagate in either direction on a general interconnect segment. Direction controls are automatically established by the Logic Cell Array development system software. Repowering buffers are provided only for the general-purpose interconnect since the direct and long line resources do not exhibit the same R-C delay accumulation. The Logic Cell Array is divided into nine sections with buffers automatically provided for general interconnect at the boundaries of these sections. These boundaries can be viewed with the development system. For routing within a section, no buffers are used. The delay calculator of the XACT development system automatically calculates and displays the block, interconnect and buffer delays for any selected paths.

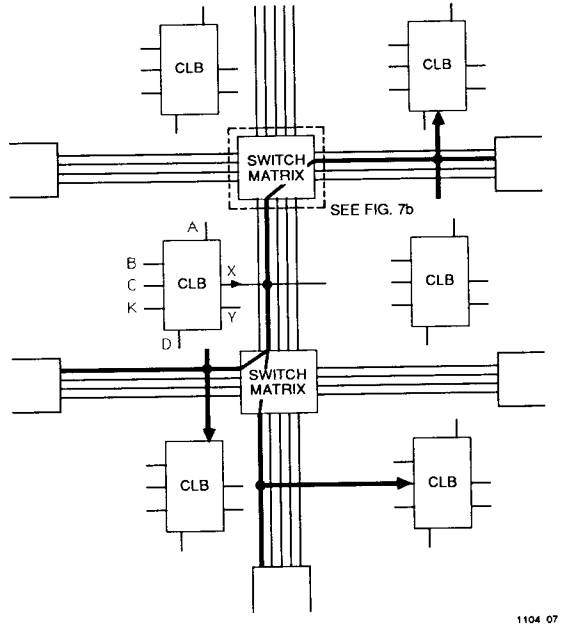


Figure 7a. General-Purpose Interconnect

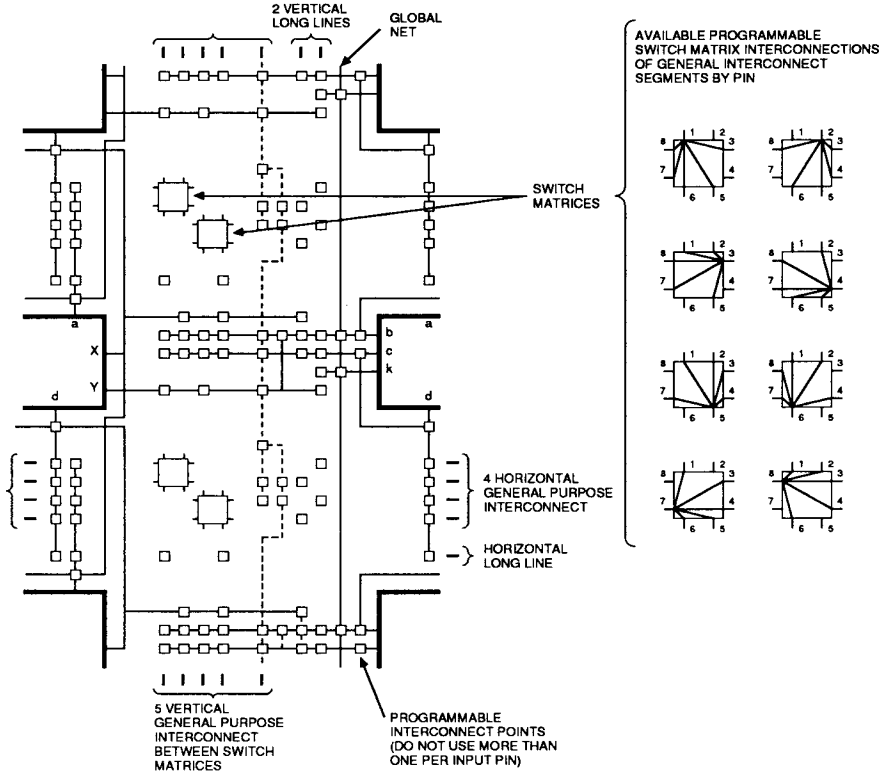


Figure 7b. Routing and Switch Matrix Connections

Long Lines

Long-lines, shown in Figure 8a, run both vertically and horizontally the height or width of the interconnect area. Each vertical interconnection column has two long lines; each horizontal row has one, with an additional long line adjacent to each set of I/O blocks. The long lines bypass the switch matrices and are intended primarily for signals that must travel a long distance or must have minimum skew among multiple destinations.

A global buffer in the Logic Cell Array is available to drive a single signal to all B and K inputs of logic blocks. Using the global buffer for a clock provides a very low skew, high fan-out synchronized clock for use at any or all of the logic blocks. At each block, a configuration bit for the K input to the block can select this global line as the storage element clock signal. Alternatively, other clock sources can be used.

A second buffer below the bottom row of the array drives a horizontal long line which, in turn, can drive a vertical long line in each interconnection column. This alternate buffer also has low skew and high fan-out capability. The network formed by this alternate buffer's long lines can be selected to drive the B, C or K inputs of the logic blocks.

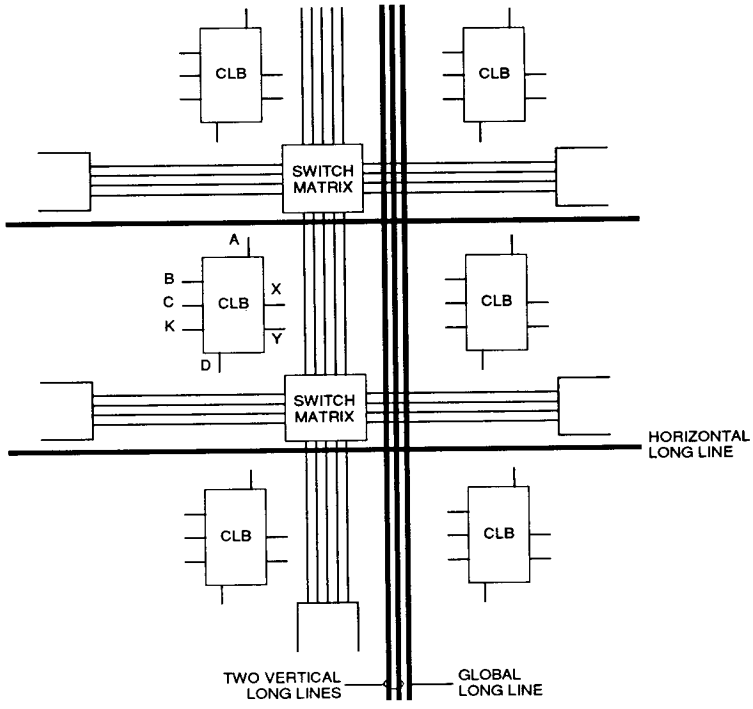


Figure 8a. Long Line Interconnect

Alternatively, these long lines can be driven by a logic or I/O block on a column by column basis. This capability provides a common, low-skew clock or control line within each column of logic blocks. Interconnections of these long lines are shown in Figure 8b.

Direct Interconnect

Direct interconnect, shown in Figure 9, provides the most efficient implementation of networks between adjacent logic or I/O blocks. Signals routed from block to block by means of direct interconnect exhibit minimum interconnect propagation and use minimum interconnect resources. For each Configurable Logic Block, the X output may be connected directly to the C or D inputs of the CLB above and to the A or B inputs of the CLB below it. The Y output can use direct interconnect to drive the B input of the block immediately to its right. Where logic blocks are adjacent to I/O blocks, direct connect is provided to the I/O block input (I) on the left edge of the die, the output (O) on the right edge, or both on I/O blocks at the top and bottom of the die. Direct interconnections of I/O blocks with CLBs are shown in Figure 8b.

CRYSTAL OSCILLATOR

An internal high speed inverting amplifier is available to implement an on-chip crystal oscillator. It is associated with the auxiliary clock buffer in the lower right corner of the die. When configured to drive the auxiliary clock buffer, two special adjacent user I/O blocks are also configured to connect the oscillator amplifier with external crystal oscillator components, as shown in Figure 10. This circuit becomes active before configuration is complete in order to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. The feedback resistor R1 between output and input, biases the amplifier at threshold. It should be as large a value as practical to minimize loading of the crystal. The inversion of the amplifier, together with the R-C networks and crystal, produce the 360-degree phase shift of the Pierce oscillator. A series resistor R2 may be included to add to

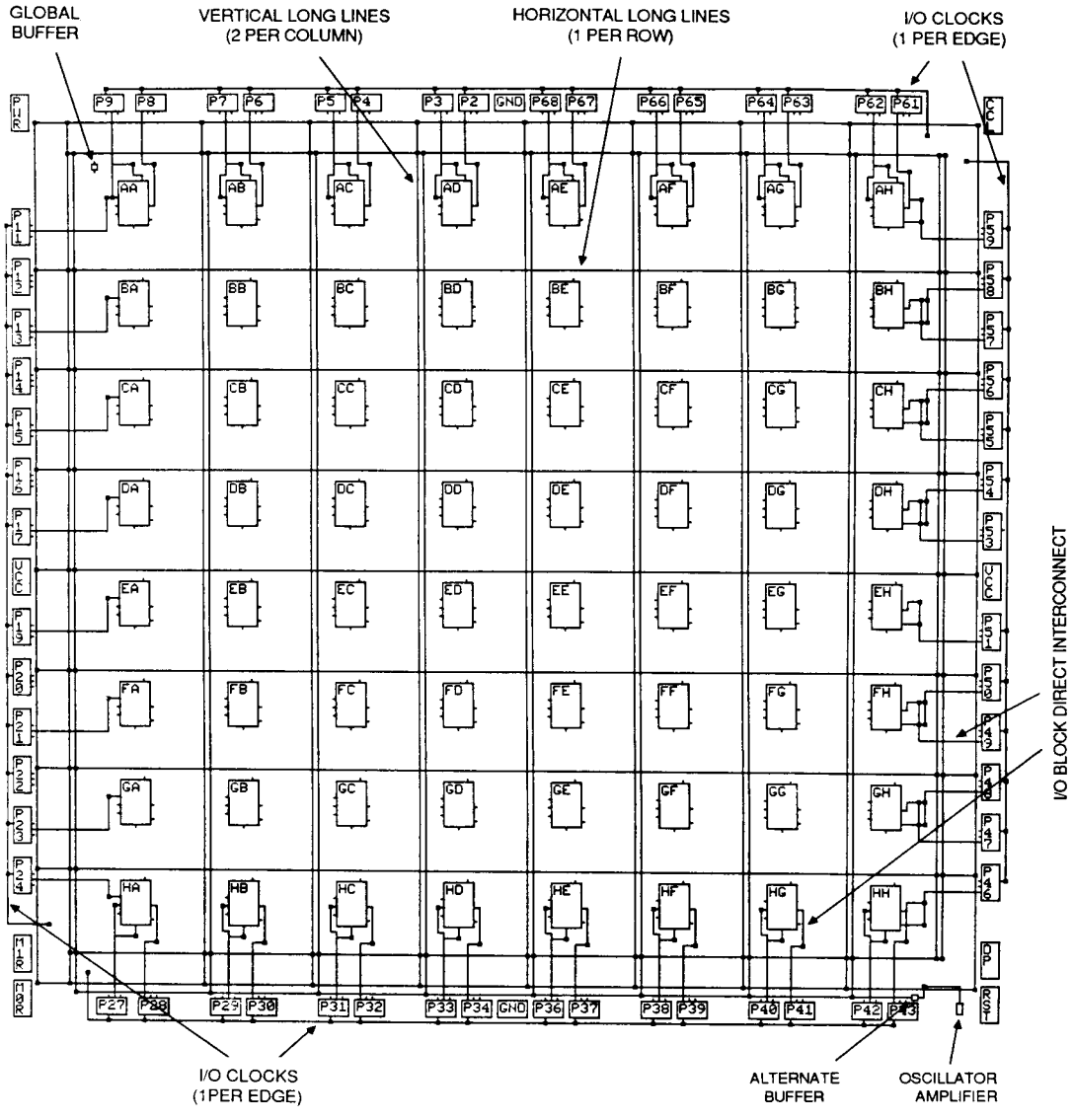


Figure 8b. XC2064 Long Lines, I/O Clocks, I/O Direct Interconnect

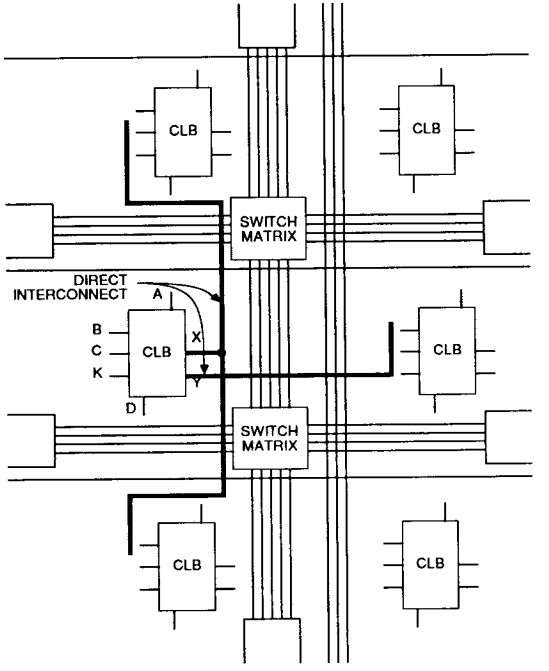
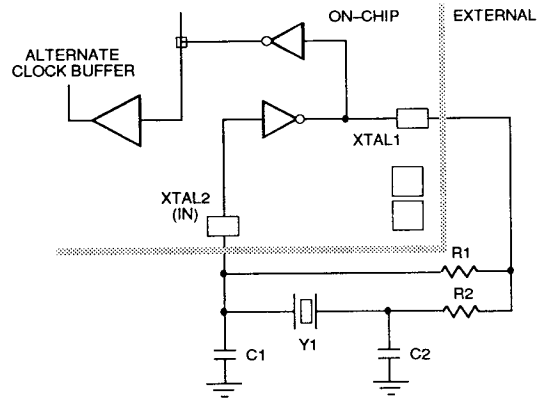


Figure 9. Direct Interconnect



SUGGESTED COMPONENT VALUES

R1 0.5 – 1 MΩ
R2 0 – 1 KΩ (may be required for low frequency, phase shift and/or compensation level for crystal Q)
C1, C2 10 – 40 pF
Y1 1 – 20 MHz AT cut series resonant

	XTAL1	XTAL2
48 DIP	33	30
68 PLCC	46	43
68 PGA	J10	L10
84 PLCC	56	53
84 PGA	K11	L11

Figure 10. Crystal Oscillator

the amplifier output impedance when needed for phase-shift control or crystal resistance matching or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be adjusted by the ratio of C2/C1. The amplifier is designed to be used over the range from 1 MHz up to one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Operation at frequencies above 20 MHz generally requires a crystal to operate in a third overtone mode, in which the fundamental frequency must be suppressed by the R-C networks. When the amplifier does not drive the auxiliary buffer, these I/O blocks and their package pins are available for general user I/O.

POWER

Power Distribution

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. For packages having more than 48 pins, two Vcc pins and two ground pins are provided (see Figure 11). Inside the LCA, a dedicated Vcc and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of Vcc and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are appropriately decoupled. Typically a 0.1 µF capacitor connected between the Vcc and ground pins near the package will provide adequate decoupling.

Output buffers capable of driving the specified 4 mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. Multiple Vcc and ground pin connections are required for package types which provide them.

Power Consumption

The Logic Cell Array exhibits the low power consumption characteristic of CMOS ICs. Only quiescent power is required for the LCA configured for CMOS input levels. The TTL input level configuration option requires additional power for level shifting. The power required by the static memory cells which hold the configuration data is very low and may be maintained in a power-down mode.

Typically most of power dissipation is produced by capacitive loads on the output buffers, since the power per output is 25 µW / pF / MHz . Another component of I/O power is the DC loading on each output pin. For any given system, the user can calculate the I/O power requirement based on the sum of capacitive and resistive loading of the devices driven by the Logic Cell Array.

Internal power supply dissipation is a function of clock frequency and the number of nodes changing on each clock. In an LCA the fraction of nodes changing on a given clock is typically low (10–20%). For example, in a 16-bit binary counter, the average clock produces a change in slightly less than 2 of the 16 bits. In a 4-input AND gate there will be 2 transitions in 16 states. Typical global clock buffer power is about 3 mW / MHz for the XC2064 and 4 mW / MHz for the XC2018. With a "typical" load of three general interconnect segments, each Configurable Logic Block output requires about 0.4 mW / MHz of its output frequency. Graphs of power versus operating frequency are shown in Table 1 on page 2-83.

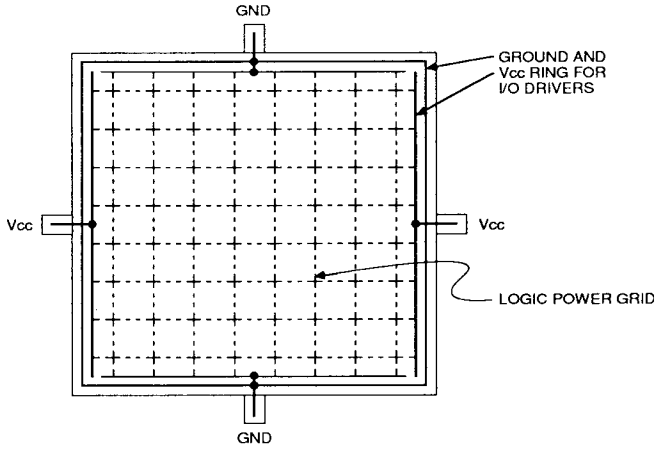


Figure 11. LCA Power Distribution

PROGRAMMING

Configuration data to define the function and interconnection within a Logic Cell Array are loaded automatically at power-up or upon command. Several methods of automatically loading the required data are designed into the Logic Cell Array and are determined by logic levels applied to mode selection pins at configuration time. The form of the data may be either serial or parallel, depending on the configuration mode. The programming data are independent of the configuration mode selected. The state diagram of Figure 12 illustrates the configuration process.

Input thresholds for user I/O pins can be selected to be either TTL-compatible or CMOS-compatible. At power-up, all inputs are TTL-compatible and remain in that state until the LCA begins operation. If the user has selected CMOS compatibility, the input thresholds are changed to CMOS levels during configuration.

Figure 13 shows the specific data arrangement for the XC2064 device. Future products will use the same data format to maintain compatibility between different devices of the Xilinx product line, but they will have different sizes and numbers of data frames. For the XC2064,

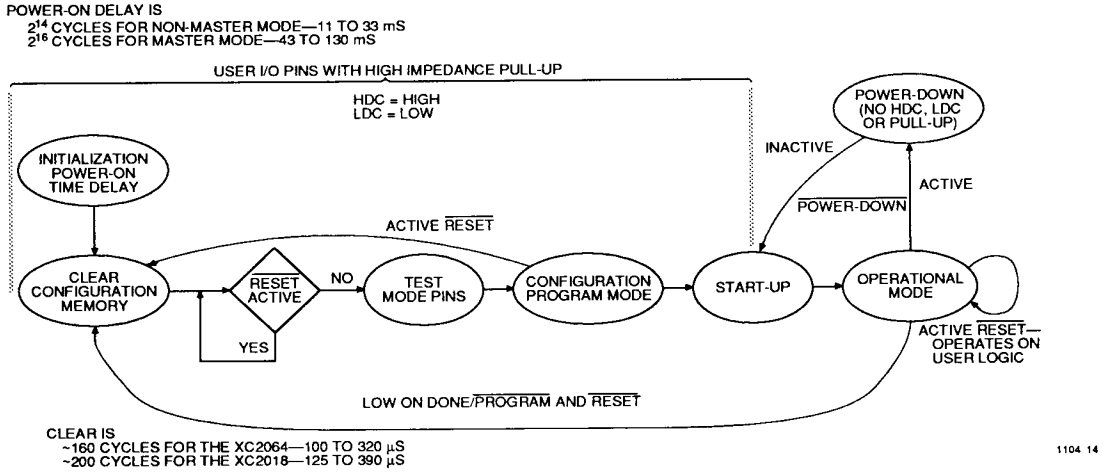


Figure 12. A State Diagram of the Configuration Process for Power-up and Re-program

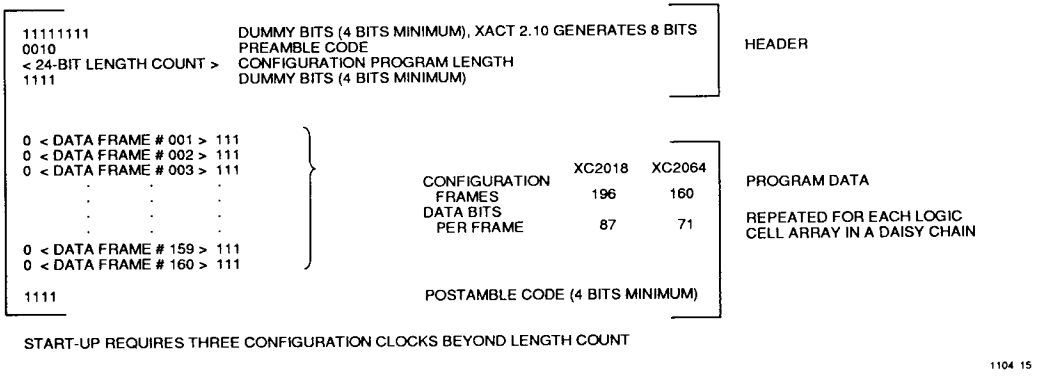


Figure 13. XC2064 Internal Configuration Data Arrangement

configuration requires 12,038 bits for each device. For the XC2018, the configuration of each device requires 17,878 bits. The XC2064 uses 160 configuration data frames and the XC2018 uses 197.

The configuration bit stream begins with preamble bits, a preamble code and a length count. The length count is loaded into the control logic of the Logic Cell Array and is used to determine the completion of the configuration process. When configuration is initiated, a 24-bit length counter is set to 0 and begins to count the total number of configuration clock cycles applied to the device. When the current length count equals the loaded length count, the configuration process is complete. Two clocks before completion, the internal logic becomes active and is reset. On the next clock, the inputs and outputs become active as configured and consideration should be given to avoid configuration signal contention. *(Attention must be paid to avoid contention on pins which are used as inputs during configuration and become outputs in operation.)* On the last configuration clock, the completion of configuration is signalled by the release of the DONE / $\overline{\text{PROG}}$ pin of the device as the device begins operation. This open-drain output can be AND-tied with multiple Logic Cell Arrays and used as an active-High READY or active-Low , $\overline{\text{RESET}}$, to other portions of the system. High during configuration (HDC) and low during configuration ($\overline{\text{LDC}}$), are released one CCLK cycle before DONE is asserted. In master mode configurations, it is convenient to use $\overline{\text{LDC}}$ as an active-Low EPROM chip enable.

As each data bit is supplied to the LCA, it is internally assembled into a data word. As each data word is completely assembled, it is loaded in parallel into one word of the internal configuration memory array. The last word must be loaded before the current length count compare is true. If the configuration data are in error, e.g., PROM address lines swapped, the LCA will not be ready at the length count and the counter will cycle through an additional complete count prior to configuration being "done".

Figure 14 shows the selection of the configuration mode based on the state of the mode pins M0 and M1. These package pins are sampled prior to the start of the configuration process to determine the mode to be used. Once configuration is DONE and subsequent operation has begun, the mode pins may be used to perform data readback, as discussed later. An additional mode pin, M2, must be defined at the start of configuration. This package pin is a user-configurable I/O after configuration is complete.

MODE PIN			MODE SELECTED
M0	M1	M2	
0	0	0	MASTER SERIAL
0	0	1	MASTER LOW MODE
0	1	1	MASTER HIGH MODE
1	0	1	PERIPHERAL MODE
1	1	1	SLAVE MODE

MASTER LOW ADDRESSES BEGIN AT 0000 AND INCREMENT
MASTER HIGH ADDRESSES BEGIN AT FFFF AND DECREMENT

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Figure 14. Configuration Mode Selection

Initialization Phase

When power is applied, an internal power-on-reset circuit is triggered. When Vcc reaches the voltage at which the LCA begins to operate (nominally 2.5 to 3 V), the chip is initialized, outputs are made high-impedance and a time-out is initiated to allow time for power to stabilize. This time-out (11 to 33 ms) is determined by a counter driven by a self-generated, internal sampling clock that drives the configuration clock (CCLK) in master configuration mode. This internal sampling clock will vary with process, temperature and power supply over the range of 0.5 to 1.5 MHz. LCAs with mode lines set for master mode will time-out of their initialization using a longer counter (43 to 130 ms) to assure that all devices, which it may be driving in a daisy chain, will be ready. Configuration using peripheral or slave modes must be delayed long enough for this initialization to be completed.

The initialization phase may be extended by asserting the active-Low external $\overline{\text{RESET}}$. If a configuration has begun, an assertion of $\overline{\text{RESET}}$ will initiate an abort, including an orderly clearing of partially loaded configuration memory bits. After about three clock cycles for synchronization, initialization will require about 160 additional cycles of the internal sampling clock (197 for the XC2018) to clear the internal memory before another configuration may begin. Reprogramming is initialized by a High-to-Low transition on $\overline{\text{RESET}}$ (after $\overline{\text{RESET}}$ has been High for at least 6 µs) followed by a Low level (for at least 6 µs) on both the $\overline{\text{RESET}}$ and the open-drain DONE/$\overline{\text{PROG}}$ pins. This returns the LCA to the CLEAR state, as shown in Fig. 12.

Master Mode

In Master mode, the Logic Cell Array automatically loads the configuration program from an external memory device. Figure 15a shows an example of the Master mode connections required. The Logic Cell Array provides 16 address outputs and the control signals $\overline{RCLK}$ (Read Clock), HDC (High during configuration) and $\overline{LDC}$ (Low during configuration) to execute Read cycles from the external memory. Parallel 8-bit data words are read and internally serialized. As each data word is read, the least significant bit of each byte, normally D0, is the next bit in the serial stream.

Addresses supplied by the Logic Cell Array can be selected by the mode lines to begin at address 0 and incremented to reach the memory (master Low mode), or they can begin at address FFFF Hex and be decremented (master High mode). This capability is provided to allow the Logic Cell Array to share external memory with another device, such as a microprocessor. For example, if the processor begins its execution from Low memory, the

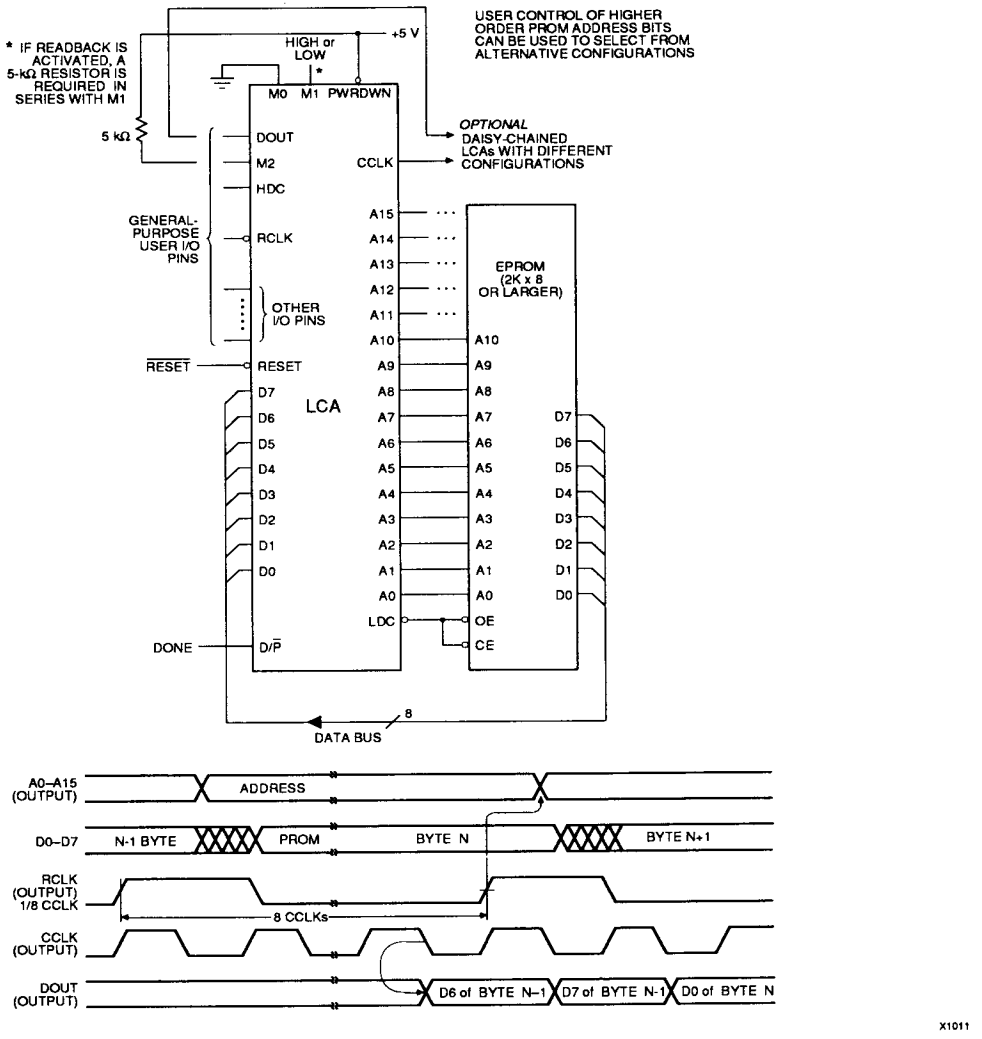

Figure 15a. Master Parallel Mode. Configuration data are loaded automaticaly from an external byte wide PROM. An XC2000 LDC signal can provide a PROM inhibit as the user I/Os become active.

Logic Cell Array can load itself from High memory and enable the processor to begin execution once configuration is completed. The Done/$\overline{PROG}$ output pin can be used to hold the processor in a Reset state until the Logic Cell Array has completed the configuration process

The Master Serial mode uses serial configuration data, synchronized by the rising edge of CCLK, as shown in Figure 15b.

Peripheral Mode (Bit Serial)

Peripheral mode provides a simplified interface through which the device may be loaded as a processor peripheral.

Figure 16 shows the peripheral mode connections. Processor Write cycles are decoded from the common assertion of the active-Low write strobe ($\overline{IOWRT}$), and two active-Low and of the active-High chip selects ($\overline{CS0}$ $\overline{CS1}$ CS2). If all these signals are not available, the unused inputs should be driven to their respective active levels. The Logic Cell Array will accept one bit of the configuration program on the data input (DIN) pin for each processor Write cycle. Data is supplied in the serial sequence described earlier.

Since only a single bit from the processor data bus is loaded per cycle, the loading process involves the processor reading a byte or word of data, writing a bit of the data to the Logic cell Array, shifting the word and writing a

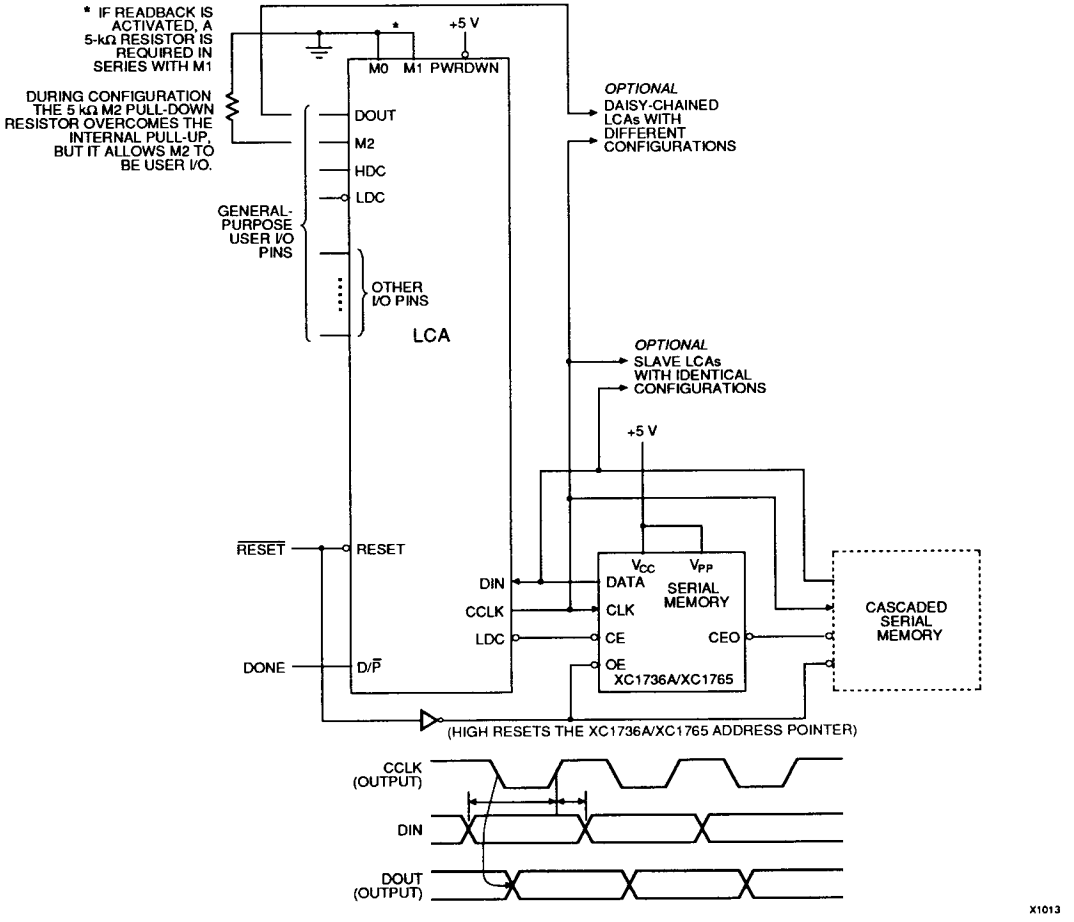

Figure 15b. Master Serial Mode. The one time programmable XC1736A Serial Configuration PROM supports automatic loading of configuration programs up to 36 Kbits. Multiple XC1736As can be cascaded to support additional LCAs. An XC2000 LDC signal can provide an XC1736A inhibit as the user I/Os become active.

bit until all bits of the word are written, then continuing in the same fashion with the next word, etc. After the configuration program has been loaded, an additional three clocks (a total of three more than the length count) must be supplied in order to complete the configuration process. When more than one device is being used in the system, each device can be assigned a different bit in the processor data bus, and multiple devices can be loaded on each processor write cycle. This "broadside" loading method provides a very easy and time-efficient method of loading several devices.

Slave Mode

Slave mode, Figure 17, provides the simplest interface for loading the Logic Cell Array configuration. Data is supplied in conjunction with a synchronizing clock. For each Low-to-High input transition of configuration clock (CCLK), the data present on the data input (DIN) pin is loaded into the internal shift register. Data may be supplied by a processor or by other special circuits. Slave mode is used for downstream devices in a daisy-chain configuration. The data for each slave LCA are supplied by the preceding LCA in the chain, and the clock is supplied by the lead device, which is configured in master or peripheral mode. After the configuration program has been loaded, an additional three clocks (a total of three more than the length count) must be supplied in order to complete the configuration process.

Daisy Chain

The daisy-chain programming mode is supported by Logic Cell Arrays in all programming modes. In master mode and peripheral mode, the LCA can act as a source of data and control for slave devices. For example, Figure 18 shows a single device in master mode, with 2 devices in slave mode. The master mode device reads the external memory and begins the configuration loading process for all of the devices.

The data begin with a preamble and a length count which are supplied to all devices at the beginning of the configuration. The length count represents the total number of cycles required to load all of the devices in the daisy chain. After loading the length count, the lead device will load its

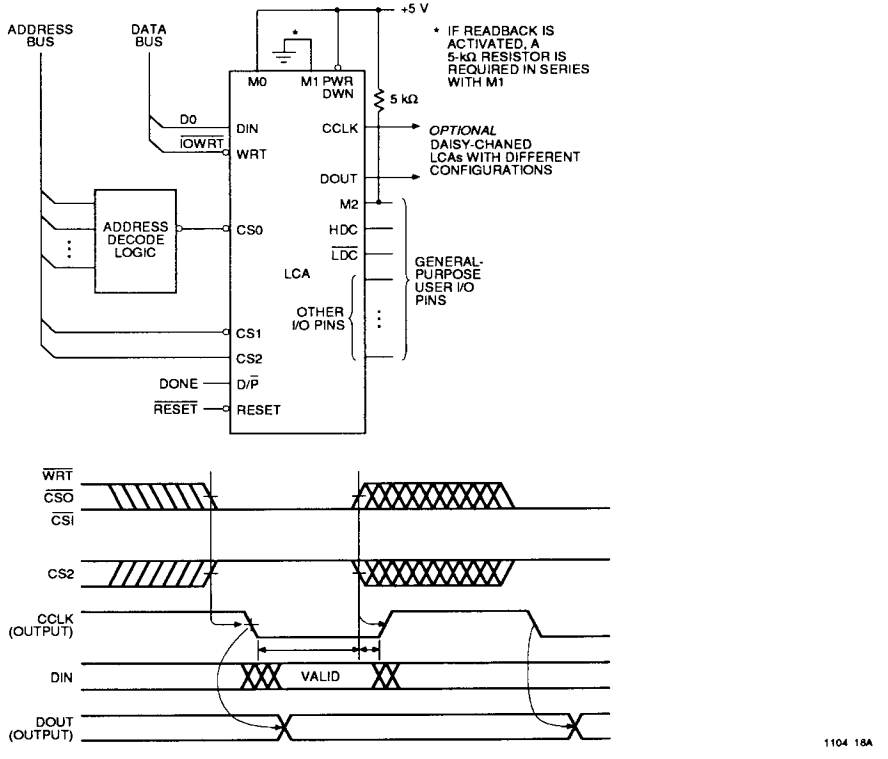

Figure 16. Peripheral Mode. Configuration data are loaded using serialized data from a microprocessor.

configuration data while providing a High DOUT to downstream devices. When the lead device has been loaded and the current length count has not reached the full value, memory access continues. Data bytes are read and serialized by the lead device. The data are passed through the lead device and appear on the data out (DOUT) pin in serial form. The lead device also generates the configuration clock (CCLK) to synchronize the serial output data. A master mode device generates an internal CCLK of 8 times the EPROM address rate, while a peripheral mode device produces CCLK from the chip select and write strobe timing.

Operation

When all of the devices have been loaded and the length count is complete, a synchronous start-up of operation is performed. On the clock cycle following the end of loading, the internal logic begins functioning in the reset state. On the next CCLK, the configured output buffers become active to allow signals to stabilize. The next CCLK cycle produces the DONE condition. The length count control of operation allows a system of multiple Logic Cell Arrays to begin operation in a synchronized fashion. If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Reprogram

The Logic Cell Array configuration memory may be rewritten while the device is operating in the user's system. The LCA returns to the Clear state where the configuration memory is cleared, I/O pins disabled, and mode lines resampled. Reprogram control is often implemented using an external open collector driver which pulls DONE/$\overline{\text{PROG}}$ LOW. Once it recognizes a stable request, the Logic Cell Array will hold DONE/$\overline{\text{PROG}}$ LOW until the new configuration has been completed. Even if the DONE/$\overline{\text{PROG}}$ pin is externally held LOW beyond the configuration period, the Logic Cell Array will begin operation upon completion of configuration. To reduce sensitivity to noise, these reprogram signals are filtered for 2–3 cycles of the LCA's internal timing generator (2 to 6 µs). Note that the Clear time-out for a Master mode reprogram or abort does not have the 4 times delay of the Initialization state. If a daisy chain is used, an external $\overline{\text{RESET}}$ is required, long enough to guarantee clearing all non-master mode devices. For XC2000-series LCA devices this is accomplished with an external time delay.

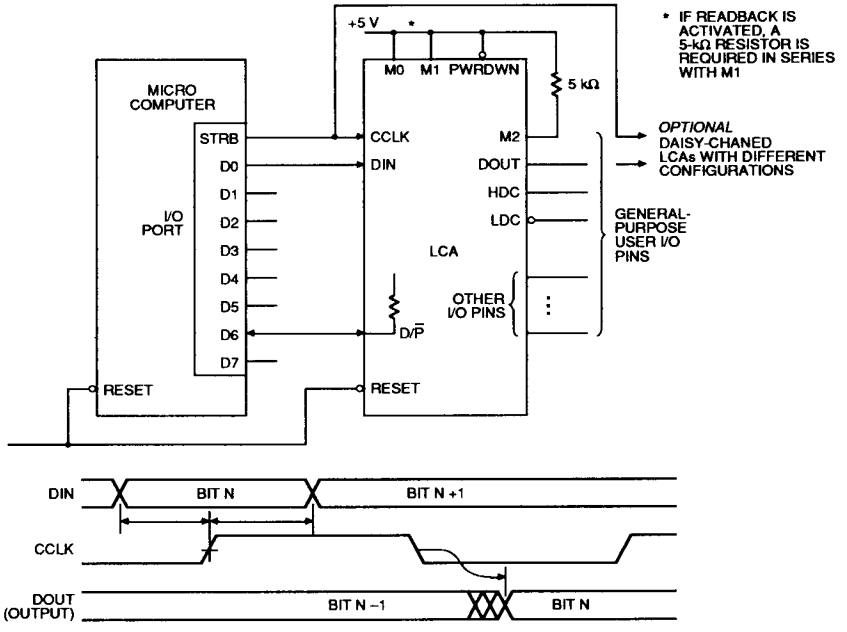

Figure 17. Slave Mode. Bit-serial configuration data are read at rising edge of the CCLK. Data on DOUT are provided on the falling edge of CCLK. Identically configured non-master mode LCAs can be configured in parallel by connecting DINs and CCLKs.

In some applications the system power supply might have momentary failures which can leave the LCA's control logic in an invalid state. There are two methods to recover from this state. The first is to cycle the Vcc supply to less than 0.1 Volt and reapply valid Vcc. The second is to provide the LCA device with simultaneous Low levels of at least 6 µs on $\overline{\text{RESET}}$ and DONE/$\overline{\text{PROG}}$ pins after the $\overline{\text{RESET}}$ pin has been High following a return to valid Vcc. This guarantees that the LCA will return to the Clear state. Either of these methods may be needed in the event of an incomplete voltage interruption. They are not needed for a normal application of power from an off condition.

Battery Backup

Because the control store of the Logic Cell Array is a CMOS static memory, its cells require only a very low standby current for data retention. In some systems, this low data retention current characteristic facilitates preserving configurations in the event of a primary power loss. The Logic Cell Array has built in power-down logic which, when activated, clears all internal flip-flops and latches, but retains the configuration. All outputs are placed in the high impedance state, and all input levels are ignored. The internal logic considers all inputs to be ones (High). Configuration is not possible during power down.

Power-down data retention is possible with a simple battery-backup circuit because the power requirement is extremely low. For retention at 2.0 V, the required current is typically on the order of 500 nA. Screening to this parameter is available. To force the Logic Cell Array into the power-down state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the Vcc pins of the package. When normal power is restored, Vcc is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The Logic Cell Array resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal I/O and logic block storage elements will be reset, the outputs will become enabled and then the DONE/$\overline{\text{PROG}}$ pin will be released. No configuration programming is involved. See Page 6-18 for further information.

SPECIAL CONFIGURATION FUNCTIONS

In addition to the normal user logic functions and interconnect, the configuration data include control for several special functions:

- Input thresholds
- Readback disable
- DONE pull-up resistor

Each of these functions is controlled by a portion of the configuration program generated by the XACT Development System.

Input Thresholds

During configuration, all input thresholds are TTL level. During configuration input thresholds are established as specified, either TTL or CMOS. The $\overline{\text{PWRDWN}}$ input threshold is an exception; it is always a CMOS level input. The TTL threshold option requires additional power for threshold shifting.

Readback

After a Logic Cell Array has been programmed, the configuration program may be read back from the device. Readback may be used for verification of configuration, and as a method of determining the state of internal logic nodes during debugging. Three Readback options are provided: on command, only once, and never.

An initiation of Readback is produced by a Low-to-High transition of the M0 / RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/$\overline{\text{RDATA}}$ (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame.

All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions. Readback data includes the state of all internal storage elements. This information is used by the Logic Cell Array development system In-Circuit Debugger to provide visibility into the internal operation of the logic while the system is operating. To read back a uniform time sample of all storage elements, it may be necessary to inhibit the system clock.

DONE Pull-up

The DONE / $\overline{\text{PROG}}$ pin is an open drain I/O that indicates programming status. As an input, it initiates a reprogram operation. An optional internal pull-up resistor may be enabled.

PERFORMANCE

The high performance of the Logic Cell Array results from its patented architectural features and from the use of an advanced high-speed CMOS manufacturing process. Performance may be measured in terms of minimum propagation times for logic elements.

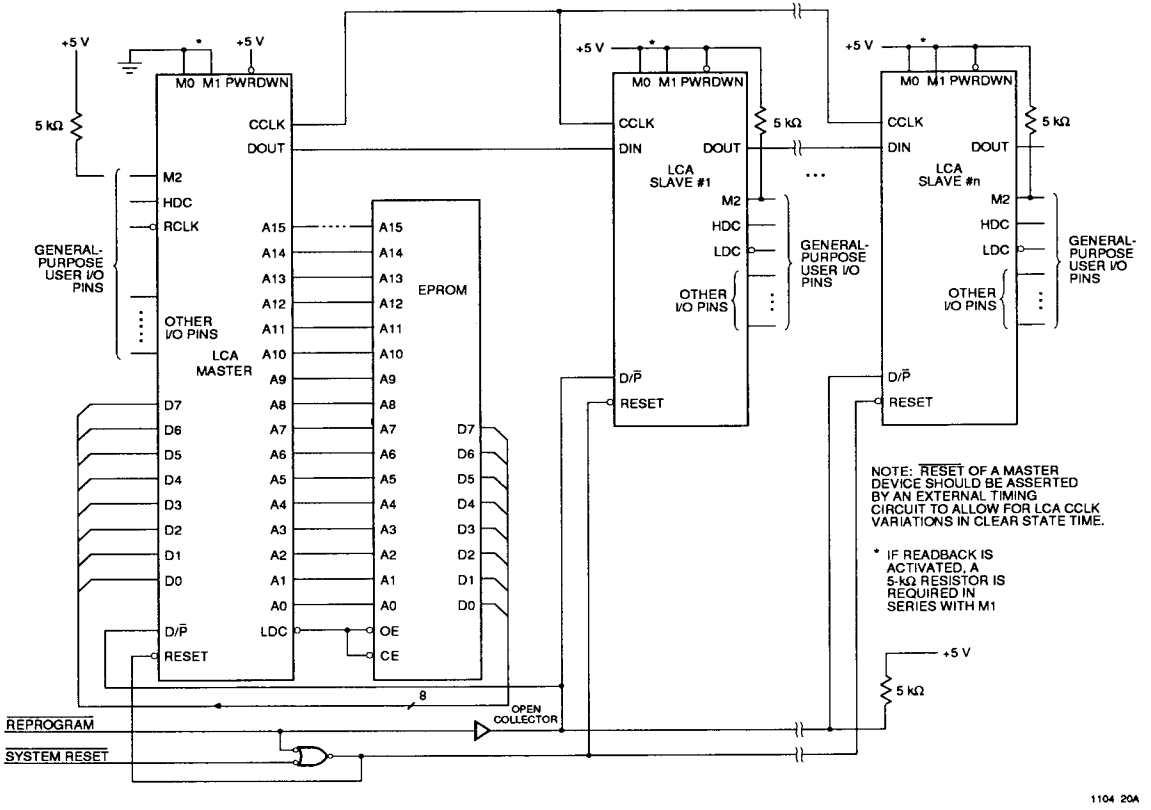

Figure 18. Master Mode Configuration with Daisy Chained Slave Mode Devices.
All are configured from the common EPROM source. A well defined termination of SYSTEM RESET is needed when controlling multiple LCAs.

Any XC3000 slave driven by an XC2000 master mode device must use "early DONE and early internal reset". (The XC2000 master will not supply the extra clock required by a "late" programmed XC3000.)

Flip-flop loop delays for the I/O block and logic block flip-flops are about 3 ns. This short delay provides very good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition which can result from assertion of the clock during data transitions. Because of the short loop delay characteristic in the LCA device, the I/O block flip-flops can be used very effectively to synchronize external signals applied to the device. Once synchronized in the I/O block, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing path delays.

Device Performance

The single parameter which most accurately describes the overall performance of the Logic Cell Array is the maximum toggle rate for a logic block storage element configured as a toggle flip-flop. The configuration for determining the toggle performance of the Logic Cell Array is shown in Figure 19. The clock for the storage element is provided by the global clock buffer and the flip-flop output Q is fed back through the combinatorial logic to form the data input for the next clock edge. Using this arrangement, flip-flops in the Logic Cell Array can be toggled at clock rates from 33–70 MHz, depending on the speed grade used.

Actual Logic Cell Array performance is determined by the critical path speed, including both the speed of the logic and storage elements in that path, and the speed of the particular network routing. Figure 20 shows a typical system logic configuration of two flip-flops with an extra combinatorial level between them. Depending on speed grade, system clock rates to 35 MHz are practical for this logic. To allow the user to make the best use of the capabilities of the device, the delay calculator in the XACT Development System determines worst-case path delays using actual impedance and loading information.

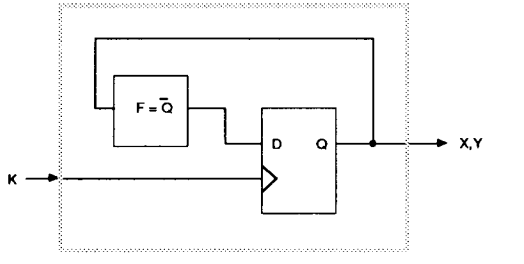

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Figure 19. Logic Block Configuration for Toggle Rate Measurement

Logic Block Performance

Logic block propagation times are measured from the interconnect point at the input of the combinatorial logic to the output of the block in the interconnect area. Combinatorial performance is independent of logic function because of the table look-up based implementation. Timing is different when the combinatorial logic is used in conjunction with the storage element. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the storage element. The delay from the clock source to the output of the logic block is critical in the timing of signals produced by storage elements. The loading on a logic block output is limited only by the additional propagation delay of the interconnect network. Performance of the logic block is a function of supply voltage and temperature, as shown in Figure 22 .

Interconnect Performance

Interconnect performance depends on the routing resource used to implement the signal path. As discussed earlier, direct interconnect from block to block provides a minimum delay path for a signal.

The single metal segment used for long lines exhibits low resistance from end to end, but relatively high capacitance. Signals driven through a programmable switch will have the additional impedance of the switch added to their normal drive impedance.

General-purpose interconnect performance depends on the number of switches and segments used, the pre-sence of the bidirectional repowering buffers and the overall loading on the signal path at all points along the path. In calculating the worst-case delay for a general interconnect path, the delay calculator portion of the XACT development system accounts for all of these elements. As an approximation, interconnect delay is proportional to the summation of totals of local metal segments beyond each programmable switch. In effect, the delay is a sum of R-C delays each approximated by an R times the total C it drives. The R of the switch and the C of the interconnect are functions of the particular device performance grade. For a string of three local interconnects, the approximate delay at the first segment, after the first switch resistance, would be three units; an additional two delay units after the next switch plus an additional delay after the last switch in the chain. The interconnect R-C chain terminates at each repowering buffer. Nearly all of the capacitance is in the interconnect metal and switches; the capacitance of the block inputs is not significant. Figure 21 shows an estimation of this delay.

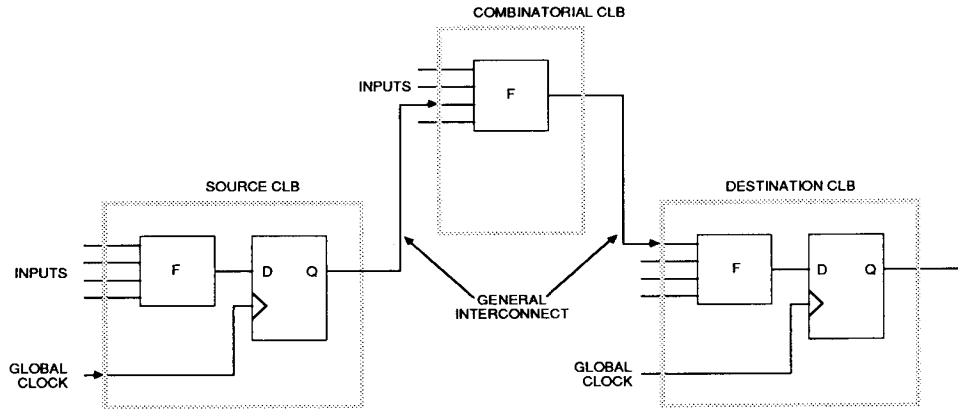

Figure 20. Typical Logic Path

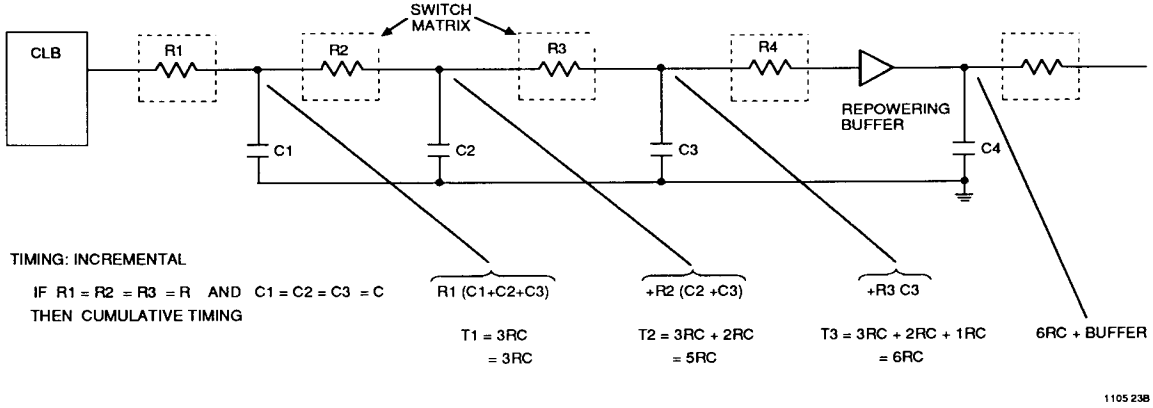

Figure 21. Interconnection Timing Example. Use of the XACT timing calculator or XACT-generated simulation model provides actual worst-case performance information.

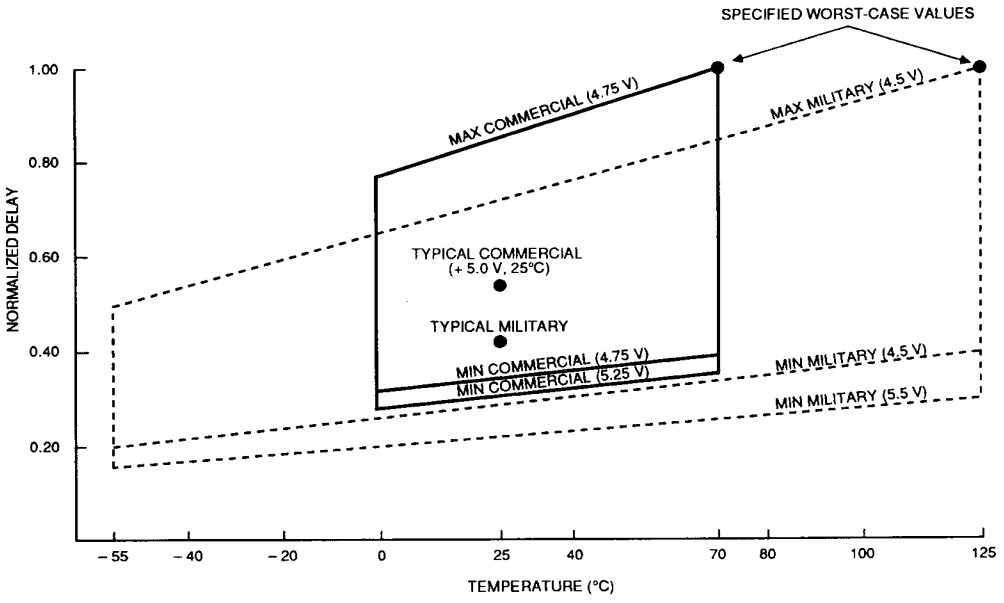

Figure 22. Relative Delay as a function of Temperature, Supply Voltage and Processing Variations.

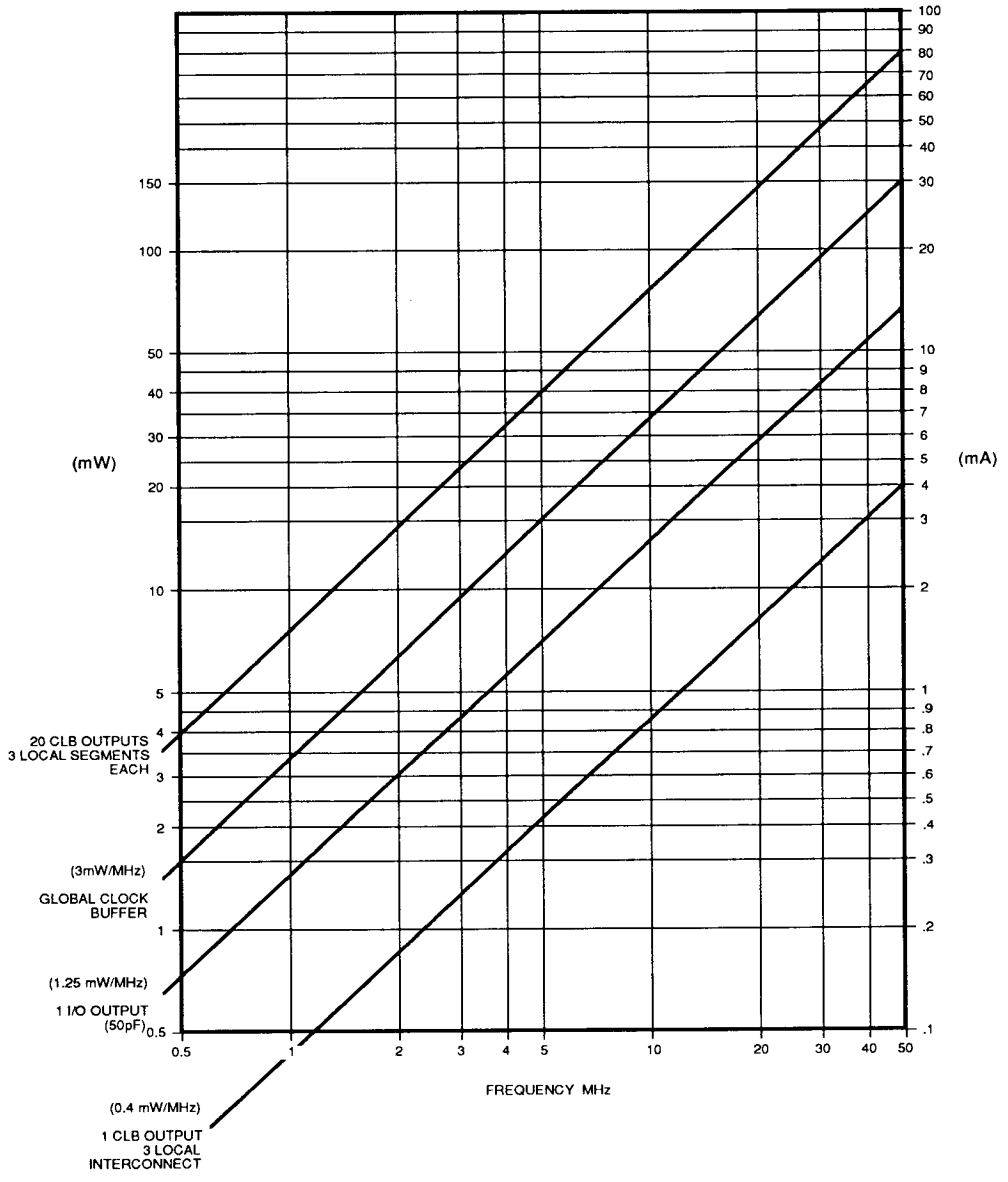

Table 1. Typical LCA Power Consumption By Element

DEVELOPMENT SYSTEMS

To accomplish hardware development support for the Logic Cell Array, Xilinx provides a development system with several options to support added capabilities. The XACT system provides the following:

- Schematic entry
- Automatic place and route
- Interactive design editing for optimization
- Interactive timing calculations
- Macro library support, both for standard Xilinx supplied functions and user defined functions
- Design entry checking for consistency and completeness
- Automatic design documentation generation
- PROM programmer format output capabilities
- Simulation interface support including automatic netlist (circuit description) and timing extraction
- Logic and timing simulation
- In-circuit design verification for multiple devices

Designing with the XACT Development System

Designing with the Logic Cell Array is similar to using conventional MSI elements or gate array cells. A range of supported packages, including FutureNet and VIEWlogic, provide schematic capture with elements from a macro library. The XACT development system then translates the schematic description into partitioned Logic Blocks and I/O Blocks, based on shared input variables or efficient use of flip-flop and combinatorial logic. Design entry can also be implemented directly with the XACT development system using an interactive graphic design editor. The design information includes both the functional specifications for each block and a definition of the interconnection networks. Automatic placement and routing is available for either method of design entry. After routing the interconnections, various checking stages and processing of that data are performed to insure that the design is correct. Design changes may be implemented in minutes. The design file is used to generate the programming data which can be down loaded directly into an LCA in the user's target system and operated. The program information may be used to program PROM, EPROM or ROM devices, or stored in some other media as needed by the final system.

PIN DESCRIPTIONS

Permanently Dedicated Pins.

V_{CC}
One or two (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
One or two (depending on package type) connections to ground. All must be connected.

$\overline{PWRDWN}$
A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. While $\overline{PWRDWN}$ is Low, V_{CC} may be reduced to any value >2.3 V. When $\overline{PWDWN}$ returns High, the LCA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. During configuration, $\overline{PWRDWN}$ must be High. If not used, $\overline{PWRDWN}$ must be tied to V_{CC}.

$\overline{RESET}$
This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{RESET}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{RESET}$ is asserted during a configuration, the LCA device is re-initialized and restarts the configuration at the termination of $\overline{RESET}$.

If $\overline{RESET}$ is asserted after configuration is complete, it provides a global asynchronous reset of all IOB and CLB storage elements of the LCA device.

$\overline{RESET}$ can also be used to recover from partial power failure. See section on Re-program under "Special Configuration Functions."

CCLK
During configuration, Configuration Clock is an output of an LCA in Master mode or Peripheral mode, but an input in Slave mode. During a Readback, CCLK is a clock input for shifting configuration data out of the LCA

CCLK drives dynamic circuitry inside the LCA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{PROG}$ (D/$\overline{P}$)
DONE is an open-drain output, configurable with or without an internal pull-up resistor. At the completion of configuration, the LCA circuitry becomes active in a synchronous order; DONE goes active High one cycle after the IOB outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the LCA and start a reconfiguration.

M0/RTRIG
As Mode 0, this input and M1, M2 are sampled before the start of configuration to establish the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{RDATA}$
As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the $\overline{RDATA}$ output.

As an active Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins that can have special functions.

M2
During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{LDC}$
During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{LDC}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MAKEBITS program.

$\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WRT}$
These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master mode,these pins become part of the parallel configuration byte, D4, D3, D2, D1. After configuration, these pins are user-programmable I/O pins.

$\overline{RCLK}$
During Master parallel mode configuration $\overline{RCLK}$ represents a "read" of an external dynamic memory device (normally not used).

D0–D7
This set of eight pins represents the parallel configuration byte for the parallel Master mode. After configuration is complete they are user programmed I/O pins.

A0–A15
During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN
During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input.

DOUT
During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.

Unrestricted User I/O Pins.

I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor of 40 to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

CONFIGURATION MODE: <M2:M1:M0>					48 DIP	68 PLCC	68 PGA	USER OPERATION
MASTER-SER <0:0:0>	SLAVE <1:1:1>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>				
GND						1	B6	GND
<<HIGH>>			A13 (O)			2	A6	I/O
			A6 (O)		1	3	B5	
			A12 (O)			4	A5	
			A7 (O)		2	5	B4	
			A11 (O)		3	6	A4	
			A8 (O)		4	7	B3	
			A10 (O)		5	8	A3	
			A9 (O)		6	9	A2	
PWRDWN (I)					7	10	B2	PWR DWN
<<HIGH>>					8	11	B1	I/O
						12	C2	
					9	13	C1	
						14	D2	
					10	15	D1	
						16	E2	
					11	17	E1	
VCC					12	18	F2	VCC
<<HIGH>>					13	19	F1	I/O
						20	G2	
					14	21	G1	
						22	H2	
					15	23	H1	
					16	24	J2	
M1 (LOW)	M1 (HIGH)	M1 (LOW)	M1 (HIGH)	M1 (LOW)	17	25	J1	RDATA (O)
M0 (LOW)	M0 (HIGH)	M0 (HIGH)	M0 (LOW)	M0 (LOW)	18	26	K1	RTRIG (I)
M2 (LOW)	M2 (HIGH)				19	27	K2	I/O
HDC (HIGH)					20	28	L2	
<<HIGH>>						29	K3	
LDC (LOW)					21	30	L3	
						31	K4	
<<HIGH>>					22	32	L4	
						33	K5	
					23	34	L5	
GND					24	35	K6	GND
						36	L6	I/O
<<HIGH>>					25	37	K7	
						38	L7	
					26	39	K8	
					27	40	L8	
			D7 (I)		28	41	K9	
			D6 (I)		29	42	L9	
RESET (I)					30	43	L10	XTL2 OR I/O
DONE (O)					31	44	K10	RESET
<<HIGH>>					32	45	K11	PROG (I)
					33	46	J10	XTL1 OR I/O
						47	J11	I/O
			D5 (I)		34	48	H10	
						49	H11	
		CSO (I)	D4 (I)		35	50	G10	
		CST (I)	D3 (I)		36	51	G11	
VCC						52	F10	VCC
						53	F11	I/O
<<HIGH>>		CS2 (I)	D2 (I)		37	54	E10	
						55	E11	
		WRT (I)	D1 (I)		38	56	D10	
RCLK			RCLK		39	57	D11	
	DIN (I)		D0 (I)		40	58	C10	
DOUT (O)					41	59	C11	
CCLK (O)	CCLK (I)	CCLK (O)			42	60	B11	CCLK (I)
			A0 (O)		43	61	B10	I/O
			A1 (O)		44	62	A10	
<<HIGH>>			A2 (O)		45	63	B9	
			A3 (O)		46	64	A9	
			A15 (O)			65	B8	
			A4 (O)		47	66	A8	
			A14 (O)			67	B7	
			A5 (O)		48	68	A7	

<<HIGH>> IS HIGH IMPEDANCE WITH A 20–50 kΩ INTERNAL PULL-UP DURING CONFIGURATION

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Table 2a. XC2064 Pin Assignments

A PLCC in a "PGA-Footprint" socket has a **different** signal pinout than a PGA device.

CONFIGURATION MODE: <M2:M1:M0>					68 PLCC	84 PLCC	84 PGA	USER OPERATION
MASTER-SER <0:0:0>	SLAVE <1:1:1>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>				
GND					1	1	C6	GND
			A13 (O)		2	2	A6	I/O
						3	A5	
						4	B5	
			A6 (O)		3	5	C5	
	<<HIGH>>		A12 (O)		4	6	A4	
			A7 (O)		5	7	B4	
			A11 (O)		6	8	A3	
			A8 (O)		7	9	A2	
			A10 (O)		8	10	B3	
			A9 (O)		9	11	A1	
PWRDWN (I)					10	12	B2	PWR DWN
					11	13	C2	I/O
					12	14	B1	
					13	15	C1	
	<<HIGH>>				14	16	D2	
					15	17	D1	
						18	E3	
					16	19	E2	
						20	E1	
					17	21	F2	
VCC					18	22	F3	VCC
					19	23	G3	I/O
						24	G1	
					20	25	G2	
	<<HIGH>>					26	F1	
					21	27	H1	
					22	28	H2	
					23	29	J1	
					24	30	K1	
M1 (LOW)	M1 (HIGH)	M1 (LOW)	M1 (HIGH)	M1 (LOW)	25	31	J2	ADATA (O)
M0 (LOW)	M0 (HIGH)	M0 (HIGH)	M0 (LOW)	M0 (LOW)	26	32	L1	RTRIG (I)
M2 (LOW)	M2 (HIGH)				27	33	K2	I/O
HDC (HIGH)					28	34	K3	
<<HIGH>>					29	35	L2	
LDC (LOW)					30	36	L3	
					31	37	K4	
					32	38	L4	
	<<HIGH>>					39	J5	
					33	40	K5	
					34	41	L5	
						42	K6	
GND					35	43	J6	GND
						44	J7	I/O
					36	45	L7	
					37	46	K7	
	<<HIGH>>				38	47	L6	
						48	L8	
					39	49	K8	
					40	50	L9	
			D7 (I)		41	51	L10	
			D6 (I)		42	52	K9	
					43	53	L11	XTL2 OR I/O
RESET (I)					44	54	K10	RESET
DONE (O)					45	55	J10	PROG (I)
					46	56	K11	XTL1 OR I/O
	<<HIGH>>				47	57	J11	I/O
			D5 (I)		48	58	H10	
						59	H11	
					49	60	F10	
						61	G10	
		CS0 (I)	D4 (I)		50	62	G11	
		CS1 (I)	D3 (I)		51	63	G9	
VCC					52	64	F9	VCC
					53	65	F11	I/O
		CS2 (I)	D2 (I)		54	66	E11	
						67	E10	
	<<HIGH>>				55	68	E9	
						69	D11	
		WRT (I)	D1 (I)		56	70	D10	
RCLK			RCLK		57	71	C11	
DIN (I)			D0 (I)		58	72	B11	
DOUT (O)					59	73	C10	
CCLK (O)	CCLK (I)	CCLK (O)			60	74	A11	CCLK (I)
			A0 (O)		61	75	B10	I/O
			A1 (O)		62	76	B9	
			A2 (O)		63	77	A10	
			A3 (O)		64	78	A9	
	<<HIGH>>		A15 (O)		65	79	B8	
			A4 (O)		66	80	A8	
			A14 (O)		67	81	B6	
						82	B7	
						83	A7	
			A5 (O)		68	84	C7	

<<HIGH>> IS HIGH IMPEDANCE WITH A 20–50 kΩ INTERNAL PULL-UP DURING CONFIGURATION

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Table 2b. XC2018 Pin Assignments

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

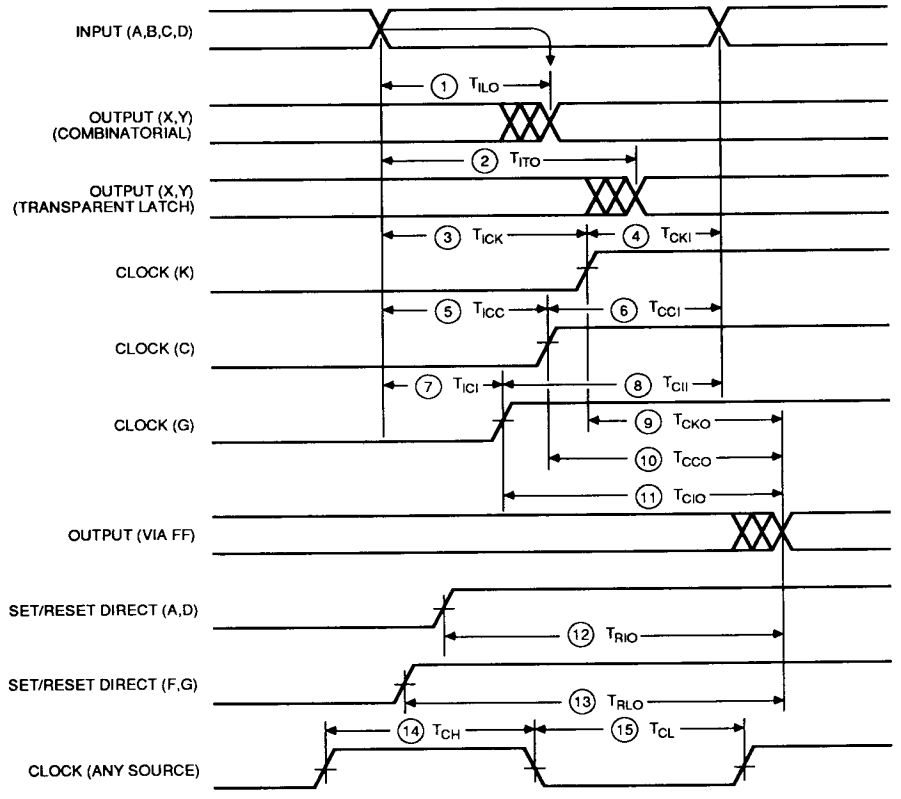
OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial –40°C to +85°C	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to +125°C	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	Vcc	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

DC CHARACTERISTICS OVER OPERATING CONDITIONS

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 ma V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 ma V_{CC} max)			0.32	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 ma V_{CC} min)	Industrial Military	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 ma V_{CC} max)			0.37	V
V_{CCPD}	Power-down supply voltage ($\overline{PWRDWN}$ must be Low)		2.3		V
I_{CCO}	Quiescent operating power supply current				
	CMOS thresholds (@ V_{CC} Max)			5	mA
	TTL thresholds (@ V_{CC} Max)			12	mA
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})			500	µA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			10 15	pF pF

CLB SWITCHING CHARACTERISTIC GUIDELINES



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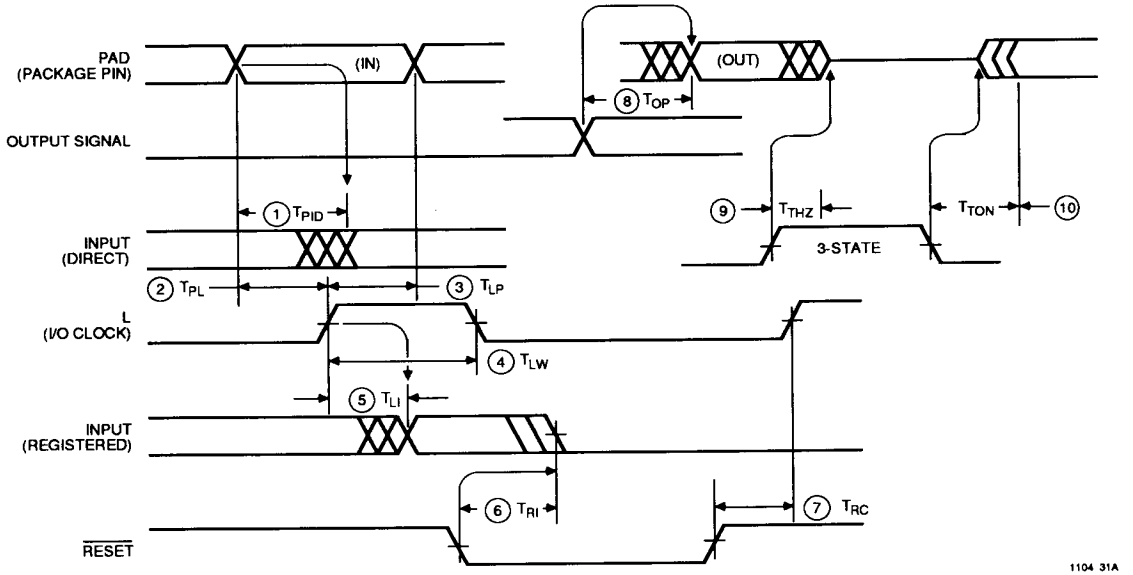
CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Speed Grade				-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
Logic Input to Output	Combinatorial Transparent latch Additional for Q through F or G to out	1 2	T_{ILO} T_{ITO} T_{QLO}		15 20 8		10 14 6		7.5 10 6	ns ns ns
K Clock	To output Logic-input setup Logic-input hold	9 3 4	T_{CKO} T_{ICK} T_{CKI}	 9 0	15	 7 0	10	 6 0	7	ns ns ns
C Clock	To output Logic-input setup Logic-input hold	10 5 6	T_{CCO} T_{ICC} T_{CCI}	 8 0	19	 6 0	13	9 5 0		ns ns ns
Logic Input to G Clock	To output Logic-input setup Logic-input hold	11 7 8	T_{CIO} T_{ICI} T_{CII}	 4 5	27	 3 4	20	 2 3	13	ns ns ns
Set/Reset direct	Input A or D to output x, y Through F or G to output Reset pad to output x, y Separation of set/reset Set/Reset pulse-width	12 13	T_{RIO} T_{RLO} T_{MRQ} T_{RS} T_{RPW}	 9 9	22 28 25	 7 7	16 21 20	 6 6	10 14 17	ns ns ns ns ns
Flip-flop Toggle rate	Q through F to flip-flop		F_{CLK}	50		70		100*		MHz
Clock	Clock High Clock Low	14 15	T_{CH} T_{CL}	8 8		7 7		5* 5*		ns ns

Notes: 1. All switching characteristics apply to all valid combinations of process, temperature and supply with a nominal chip power dissipation of 250 mW.

* These parameters are for clock pulses generated within a CLB. For an externally generated pulse, derate these parameters by 20%.

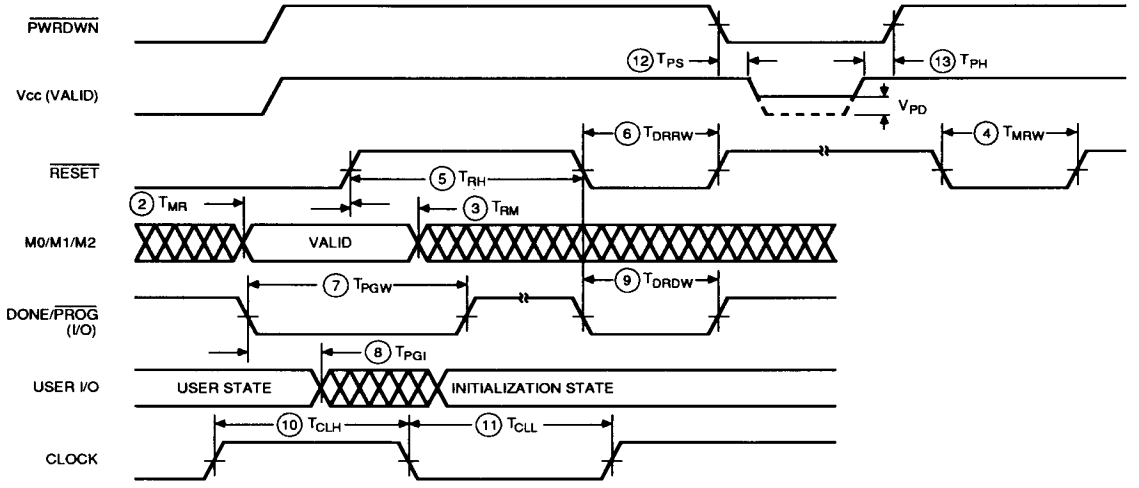
IOB SWITCHING GUIDELINES



	Description	Symbol		Speed Grade -50 Min	-50 Max	-70 Min	-70 Max	-100 Min	-100 Max	Units
Pad (package pin)	To input (direct)	1	T_{PID}		8		6		4	ns
I/O Clock	To input (storage)	5	T_{LI}		15		11		8	ns
	To pad-input setup	2	T_{PL}	8		6		4		ns
	To pad-input hold	3	T_{LP}	0		0		0		ns
	Pulse width	4	T_{LW}	9		7		5*		ns
	Frequency			50		70		100*		MHz
Output	To pad (output enabled)	8	T_{OP}		12		9		7	ns
Three-state	To pad begin hi-Z	9	T_{THZ}		20		15		11	ns
	To pad end hi-Z	10	T_{TON}		20		15		13	ns
$\overline{RESET}$	To input (storage)	6	T_{RI}		30		25		17	ns
	To input clock	7	T_{RC}	25		20		14		ns

Note: Timing is measured at 0.5 Vcc levels with 50 pF output load.
*These parameters are for clock pulses generated within an LCA. For an externally applied clock, derate these parameters by 20%.

GENERAL LCA SWITCHING CHARACTERISTIC



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	Speed Grade			-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RESET[2]	M2, M1, M0 setup	2	T_{MR}	60		60		60		ns
	M2, M1, M0 hold	3	T_{RM}	60		60		60		ns
	Width—FF Reset	4	T_{MRW}	150		150		150		ns
	High before RESET[4]	5	T_{RH}	6		6		6		µs
	Device Reset[4]	6	T_{DRRW}	6		6		6		µs
DONE/PROG	Progam width (Low)	7	T_{PGW}	6		6		6		µs
	Initialization	8	T_{PGI}		7		7		7	µs
	Device Reset [4]	9	T_{DRDW}	6		6		6		µs
CLOCK	Clock (High)	10	T_{CLH}	8		7		5		ns
	Clock (Low)	11	T_{CLL}	8		7		5		ns

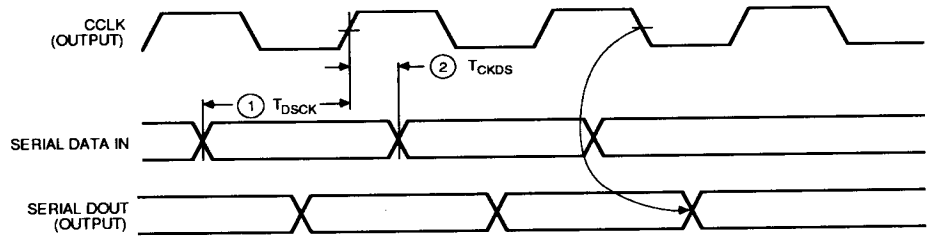
Notes: 1. At power-up, Vcc must rise from 2.0 Volts to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after Vcc has reached 4.0 V.

2. RESET timing relative to power-on and valid mode lines (M0, M1, M2) is relevant only when RESET is used to delay configuration.

3. Minimum CLOCK widths for the auxillary buffer are 1.25 times the T_{CLH}, T_{CLL}.

4. After RESET is High, RESET = D/P = Low for 6 µs will abort to CLEAR.

MASTER SERIAL MODE PROGRAMMING SWITCHING CHARACTERISTICS

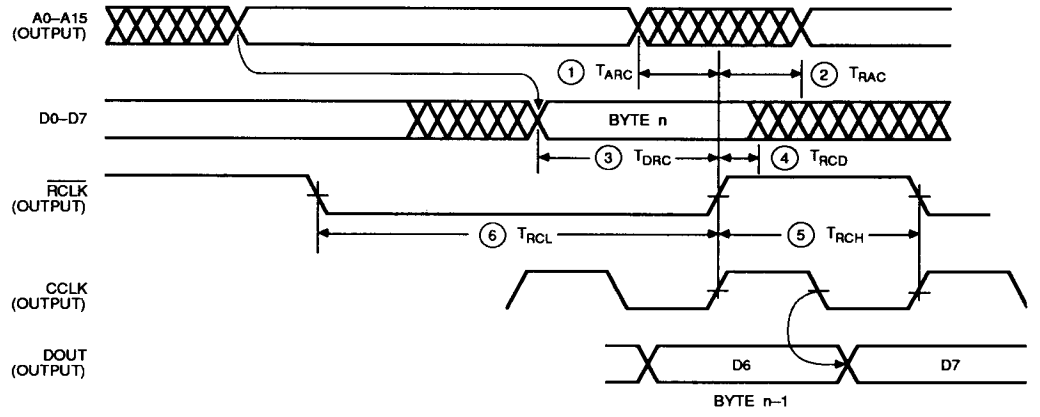


Speed Grade				-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
CCLK[2]	Data In setup	1	T_{DSCK}	60		60		60		ns
	Data In hold	2	T_{CKDS}	0		0		0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 Volts to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a >1-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after Vcc has reached 4.0 V.

2. Master-serial-mode timing is based on slave-mode testing.

MASTER PARALLEL MODE PROGRAMMING SWITCHING CHARACTERISTICS



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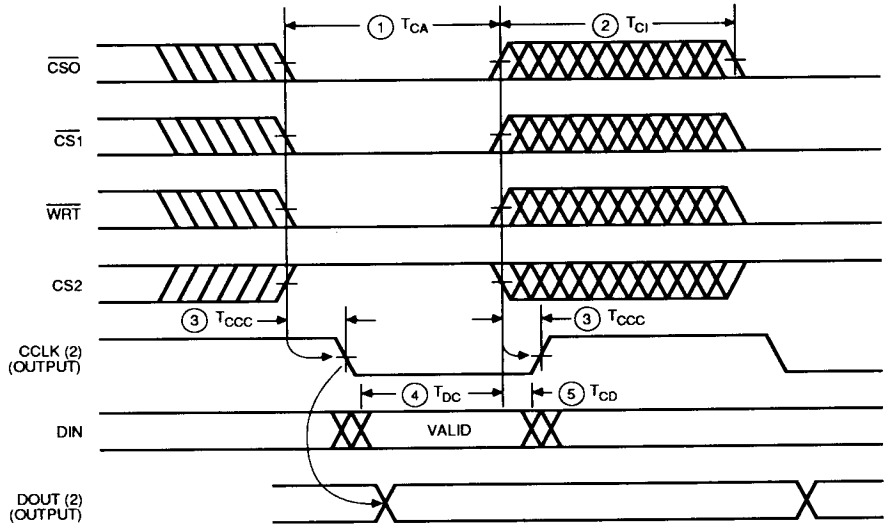
	Speed Grade			-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RCLK	From address invalid	1	T_{ARC}		0		0		0	ns
	To address valid	2	T_{RAC}		200		200		200	ns
	To data setup	3	T_{DRC}	60		60		60		ns
	To data hold	4	T_{RCD}	0		0		0		ns
	$\overline{RCLK}$ high	5	T_{RCH}	600		600		600		ns
	$\overline{RCLK}$ low	6	T_{RCL}	4.0		4.0				µs

Note: 1. CCLK and DOUT timing are the same as for slave mode.

2. At power-up, Vcc must rise from 2.0 Volts to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a >1-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after Vcc has reached 4.0 V.

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 4000 ns, EPROM data output has no hold time requirement

PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS



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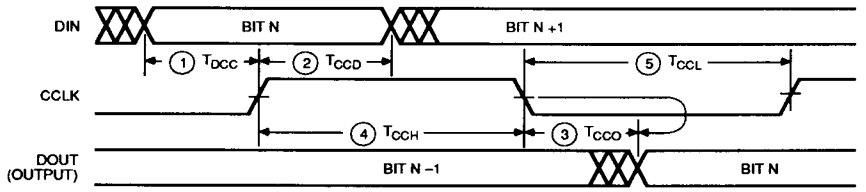
Speed Grade				-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
Controls[1] ($\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WRT}$)	Active (last active input to first inactive)	1	T_{CA}	0.25	5.0	0.25	5.0	0.25	5.0	µs
	Inactive (first inactive input to last active)	2	T_{CI}	0.25		0.25		0.25		µs
	CCLK[2]	3	T_{CCC}		75		75		75	ns
	DIN setup	4	T_{DC}	50		50		50		ns
	DIN hold	5	T_{CD}	0		0		0		ns

Notes: 1. Peripheral mode timing determined from last control signal of the logical AND of ($\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WRT}$) to transition to active or inactive state.

2. CCLK and DOUT timing are the same as for slave mode.

3. At power-up, Vcc must rise from 2.0 Volts to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a >1-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after Vcc has reached 4.0 V.

SLAVE MODE PROGRAMMING SWITCHING CHARACTERISTICS



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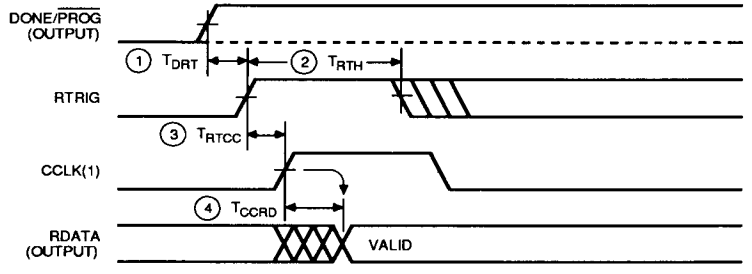
	Speed Grade			-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
CCLK	To DOUT	3	T_{CCO}		65		65		65	ns
	DIN setup	1	T_{DCC}	10		10		10		ns
	DIN hold	2	T_{CCD}	40		40		40		ns
	High time	4	T_{CCH}	0.25		0.25		0.25		µs
	Low time	5	T_{CCL}	0.25	5.0	0.25	5.0	0.25	5.0	µs
	Frequency		F_{CC}		2		2		2	MHz

Note: At power-up, Vcc must rise from 2.0 Volts to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a >1-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after Vcc has reached 4.0 V.

PROGRAM READBACK SWITCHING CHARACTERISTICS



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	Speed Grade			-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RTRIG	PROG setup	1	T_{DRT}	300		300		300		ns
	RTRIG high	2	T_{RTH}	250		250		250		ns
CCLK	RTRIG setup	3	T_{RTCC}	100		100		100		ns
	RDATA delay	4	T_{CCRD}		100		100		100	ns

Notes: 1. CCLK and DOUT timing are the same as for slave mode.
2. DONE/$\overline{\text{PROG}}$ output/input must be HIGH (device programmed) prior to a positive transition of RTRIG (M0).

COMPONENT AVAILABILITY (9/91)

		44 PIN	48 PIN		68 PIN		84 PIN		100 PIN		132 PIN		160 PIN	164 PIN	175 PIN	
		PLASTIC PLCC	PLASTIC DIP	CERAMIC DIP	PLASTIC PLCC	CERAMIC PGA	PLASTIC PCC	CERAMIC PGA	PLASTIC PQFP	CERAMIC CQFP	PLASTIC PGA	CERAMIC PGA	PLASTIC PQFP	CERAMIC CQFP	PLASTIC PGA	CERAMIC PGA
		PC44	PD48	CD48	PC68	PG68	PC84	PG84	PQ100	CQ100	PP132	PG132	PQ160	CQ164	PP175	PG175
XC2064	-50		C	I	CI	CIM										
	-70				CI	CIM										
	-100				C	C										
XC2018	-33							MB								
	-50				CI		CI	CIMB								
	-70				CI		CI	CIMB								
	-100				C		C	C								
XC3020	-50				CI		CI	CIMB	CI	CIMB						
	-70				CI		CI	CIMB	CI	CIMB						
	-100				CI		CI	CI	C	C						
	-125				C		C	C	C							
XC3030	-50	CI			CI		CI	CIM	C							
	-70	CI			CI		CI	CIM	CI							
	-100	C			CI		CI	CI	C							
	-125	C			C		C	C	C							
XC3042	-50						CI	CIMB	C	CMB	CI	CIMB				
	-70						CI	CIMB	CI	CMB	CI	CI				
	-100						CI	CI	CI	C	CI	CI				
	-125						C	C	C		C	C				
XC3064	-50						C				CI	CIM	C			
	-70						C				CI	CIM	C			
	-100						CI				CI	CI	C			
	-125						C				C	C	C			
XC3090	-50						CI						CI	CMB	CI	CIMB
	-70						CI						CI	CMB	CI	CIMB
	-100						CI						CI	C	CI	CI
	-125						C						C		C	C

X1104A

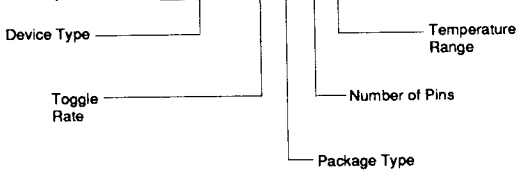
XC1736A/XC1765-PD8C Plastic 8-Pin Mini-DIP
–40°C to 85°C
XC1736A/XC1765-CD8M Ceramic 8-Pin Mini-DIP
–55°C to 125°C

LCA Temperature Options

Symbol	Description	Temperature
C	Commercial	0°C to 70°C
I	Industrial	–40°C to 85°C
M	Mil Temp	–55°C to 125°C
B	Military	MIL-STD-883, Class B

ORDERING INFORMATION

Example: **XC2064-70PC68C**



COMPATIBLE PACKAGE OPTIONS

A range of LCA devices is available in identical packages with identical pin-outs. A design can thus be started with one device, then migrated to a larger or smaller chip while retaining the original footprint and PC-board layout.

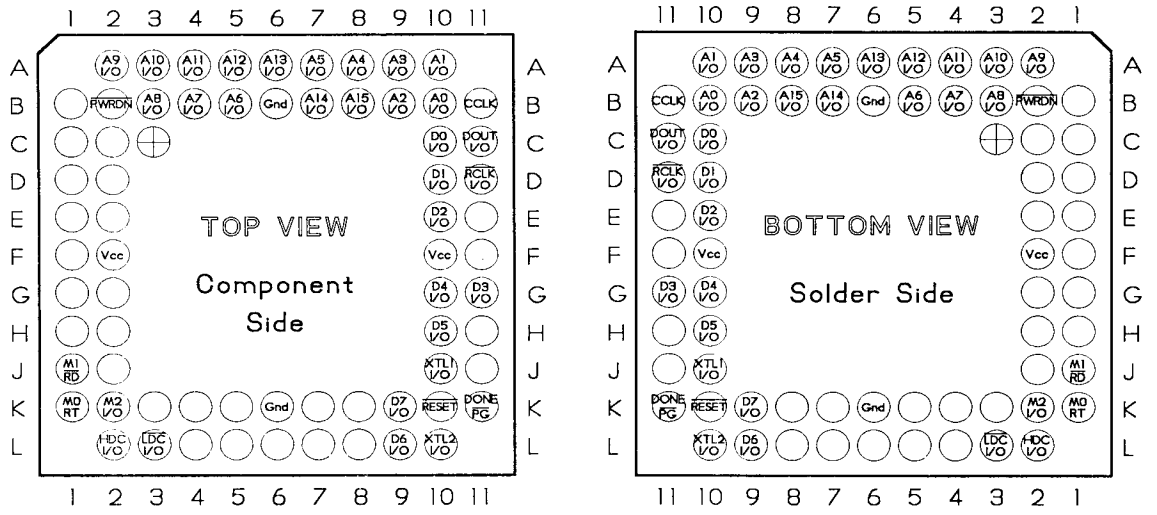
Examples:
PC 68: 2064-2018-3020-3030
PC 84: 2018-3020-3030-3042-3064-3090
PG 84: 2018-3020-3030-3042
PQ 100: 3020-3030-3042
PG 132: 3042-3064
PQ 160: 3064-3090

Note, however, that the XC2000 and XC3000 families differ in the position of XTL1 as well as three parallel address bits (6, 7 and 11) and most of the data pins used in parallel master mode.

XC2018 and XC3020 are not available in PGA68, since the PGA84 is the same size and offers more I/O.

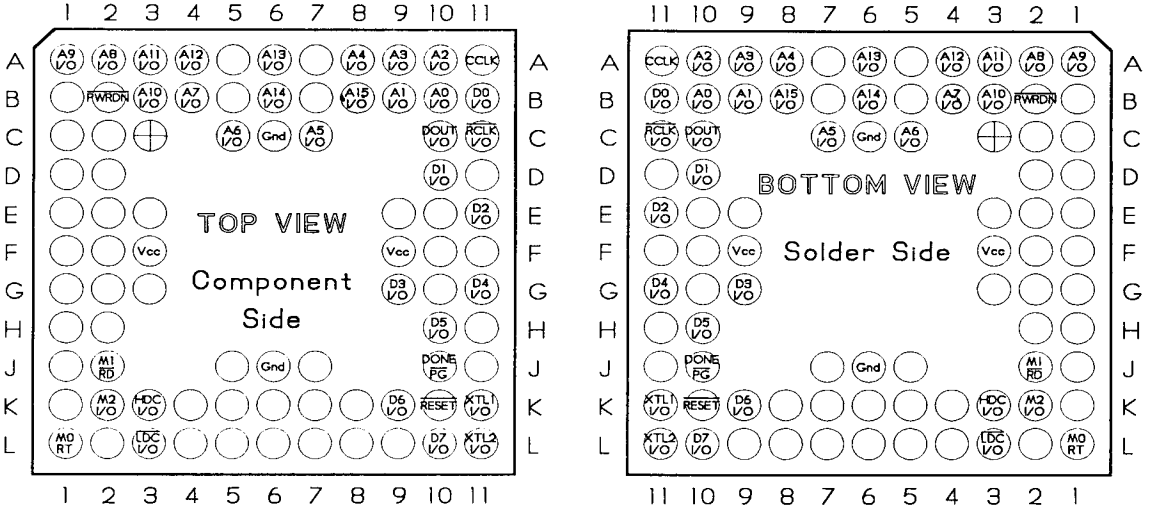
Note that a PLCC in a socket with PGA footprint generates a printed circuit board pin-out **different** from a PGA device.

PGA PIN-OUTS



⊕ = Index pin which may or may not be electrically connected to pin C2
unlabeled pin = unrestricted I/O pin

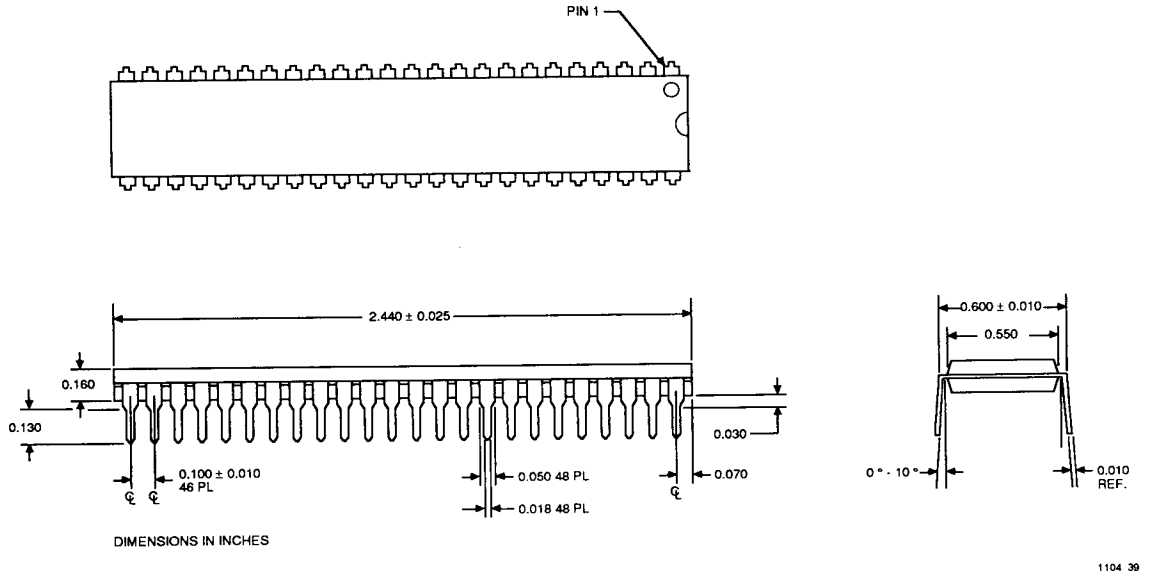
PG68 Pin-outs–XC2064



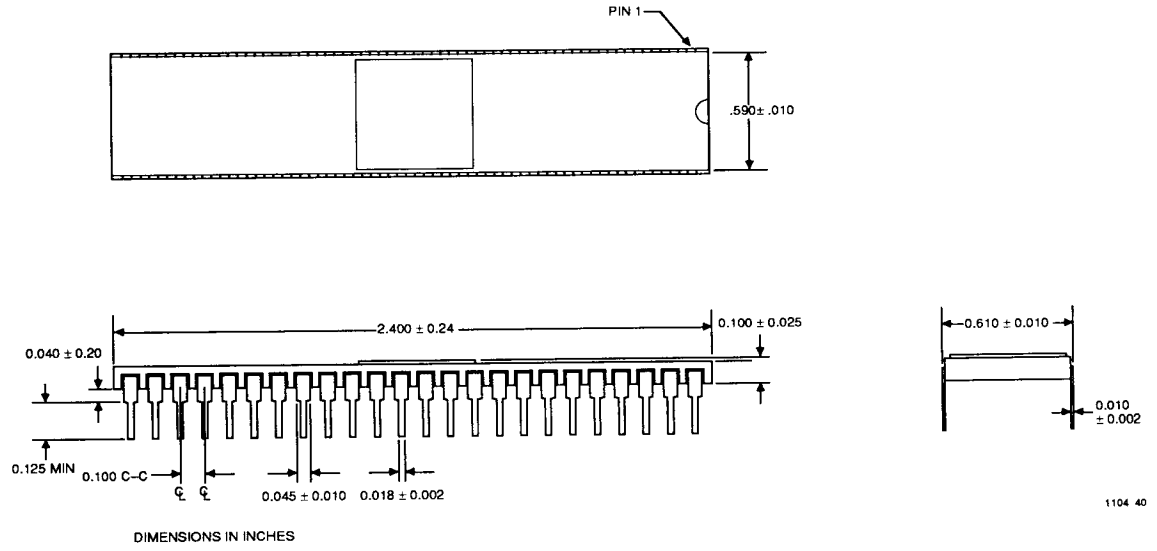
⊕ = Index pin which may or may not be electrically connected to pin C2
unlabeled pin = unrestricted I/O pin

PG84 Pin-outs–XC2018

PHYSICAL DIMENSIONS

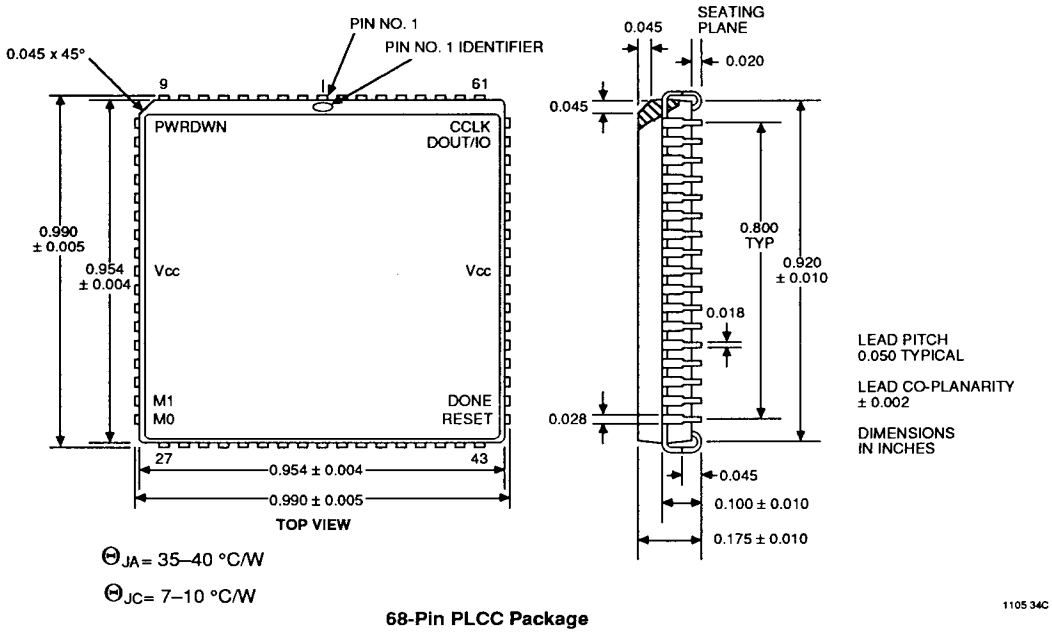


48-Pin Plastic DIP Package

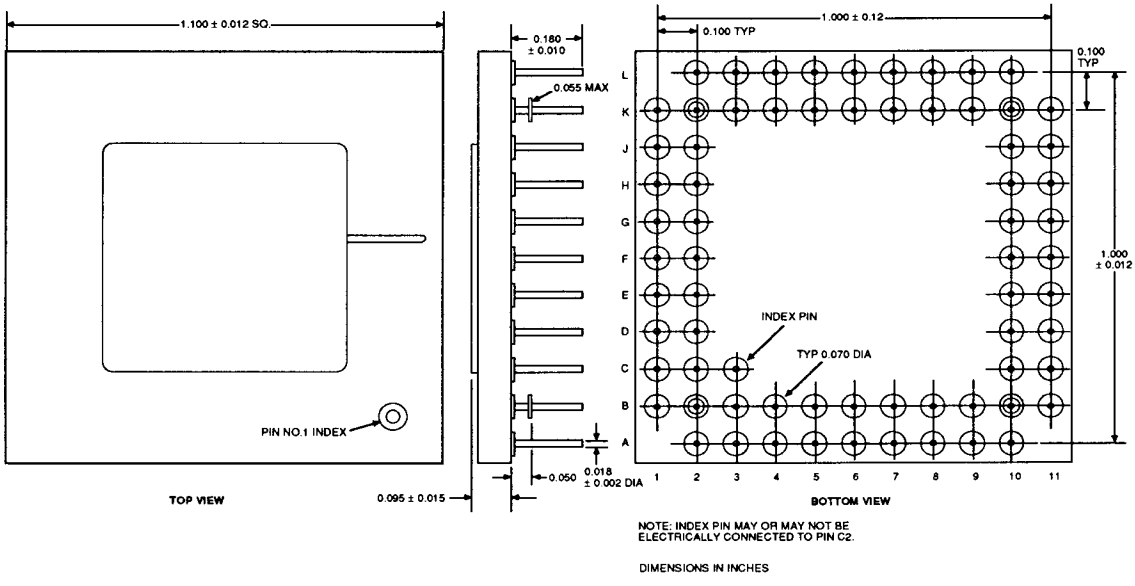


48-Pin Ceramic DIP Package

PHYSICAL DIMENSIONS (Continued)

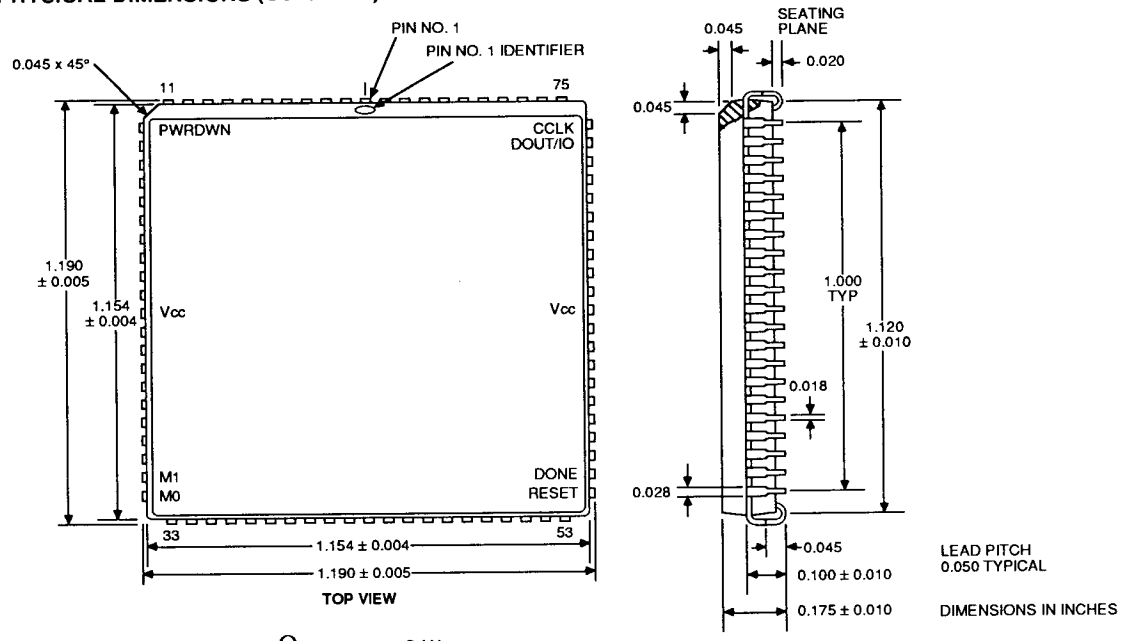


68-Pin PLCC Package

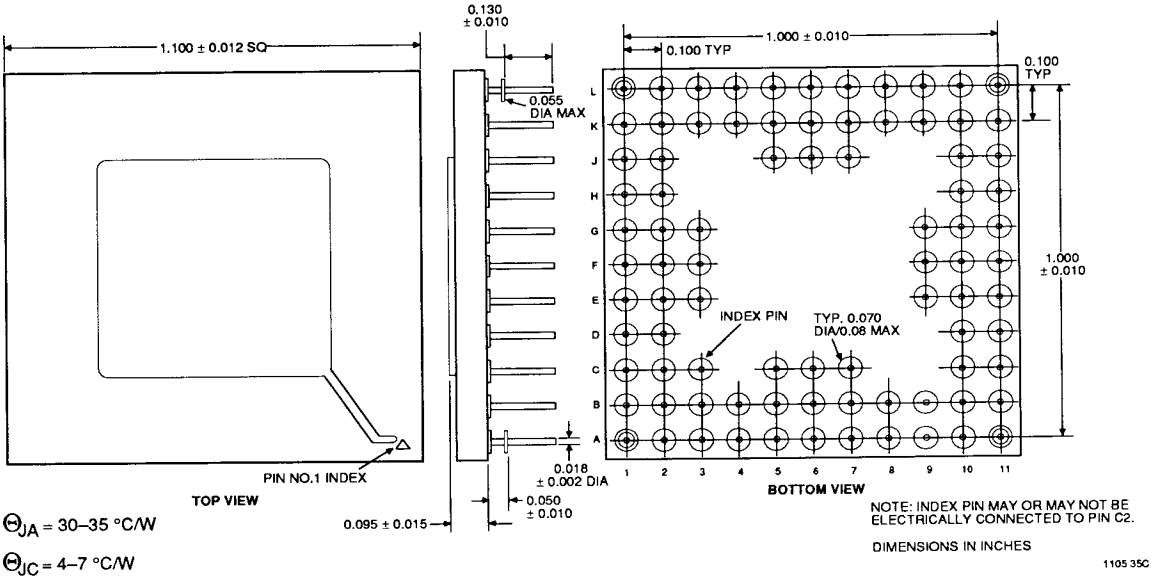


68-Pin PGA Package

PHYSICAL DIMENSIONS (Continued)



84-Pin PLCC Package



84-Pin PGA Package