REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	02-05-10	Raymond Monnin

REV	A	A	A	A	A	A														
SHEET	35	36	37	38	39	40														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
97-06-27

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-97522**

SHEET 1 OF 40

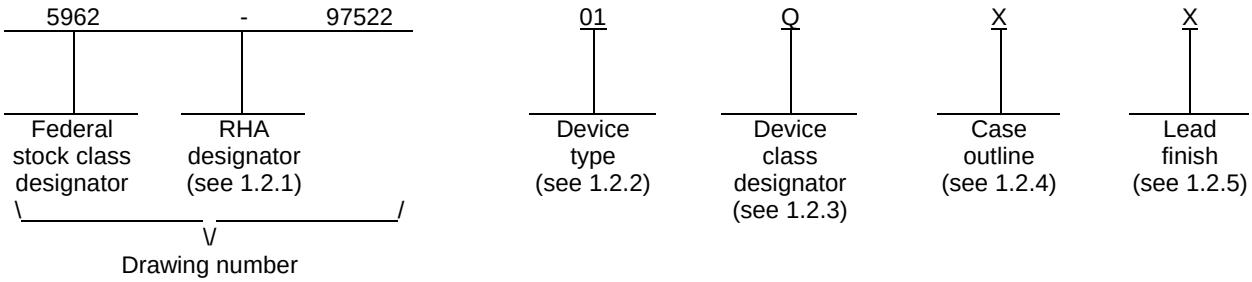
DSCC FORM 2233
APR 97

5962-E387-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	4005E-4	5000 gate programmable array	4 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA8-P156	156 1/	Pin grid array package
Y	see figure 1	164	Quad flat package
Z	see figure 1	164	Quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ 156 = actual number of pins used, not maximum listed in MIL-STD-1835.

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} +0.5 V dc
Voltage applied to three-state output (V_{TS})	-0.5 V dc to V_{CC} +0.5 V dc
Lead temperature (soldering, 10 seconds)	+260°C
Power dissipation (P_D)	2.0 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outlines Y and Z	20°C/W 3/
Junction temperature (T_J)	+150°C 4/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage relative to ground (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS}.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD 78 - IC Latch-Up Test.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 5 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA	1, 2, 3	All	2.4		V
Low level output voltage 1/	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 12 mA	1, 2, 3	All		0.4	V
Dynamic power consumption 2/ 3/		V_{CC} = 5.5 V	1, 2, 3	All		2/	mW/ MHz
Quiescent LCA supply current 4/	I_{CCO}	$V_{CC} = V_{IN}$ = 5.5 V	1, 2, 3	All		50	mA
Input leakage current	I_{IL}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	+10	µA
Output leakage current	I_{OL}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V with no load	1, 2, 3	All	-1.0	+1.0	mA
Pad pull-up current (when selected)	I_{RIN}	V_{IN} = 0 V	1, 2, 3	All	-0.2	-0.25	mA
Horizontal long line pull-up current (when selected)	I_{RLL}	At logic low	1, 2, 3	All	0.2	2.5	mA
Input capacitance	C_{IN}	See 4.4.1e	4	All		16	pF
Output capacitance	C_{OUT}	See 4.4.1e	4	All		16	pF
Functional test	FT	See 4.4.1c	7, 8A, 8B	All			
$T_{pid} + 14*T_{ilo} + Int. + T_{ops} + rtd$	t_{B1}		9, 10, 11	01		75.7	ns
$T_{pid} + 14*T_{hho} + Int. + T_{ops} + rtd$	t_{B2}					89.7	
$T_{pid} + 14*T_{iho} + Int. + T_{ops} + rtd$	t_{B3}					103.7	
$T_{pid} + 14*T_{rio} + Int. + T_{ops} + rtd$	t_{B4}					127.5	
$T_{cko} + Int. + T_{ick}$	t_{B5}				10.1		
$T_{cko} + Int. + T_{hhck}$	t_{B6}				11.1		
$T_{cko} + Int. + T_{dick}$	t_{B7}				9.1		
$T_{cko} + Int. + T_{ihck}$	t_{B8}				12.2		
$T_{cko} + Int. + T_{ecck}$	t_{B9}				10.1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Interconnect + t_{pid} + t_{ops} + t_{opcy} + t_{sum} + t_{BYP}	t_{B10}		9, 10, 11	01		140.7	ns
Interconnect + t_{pid} + t_{ops} + t_{ascy} + t_{sum} -t_{BYP}	t_{B11}					173	
Interconnect + t_{pid} + t_{ops} + t_{incy} + t_{sum}	t_{B12}					80.1	
Interconnect + t_{pid} + t_{ops} + t_{incy} + t_{BYP}	t_{B13}					57.5	
WIDE DECODER SWITCHING CHARACTERISTICS							
Full length, both pull-ups inputs from IOB I-pins	T_{WAF}	See figures 4 and 5 as applicable. 5/	3/	01		9.5	ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}		3/			12.5	
Half length, one pull-up inputs from IOB I-pins	T_{WAO}		3/			10.5	
Half length, one pull-up inputs from internal logic	T_{WAOL}		3/			12.5	
CLB SWITCHING CHARACTERISTICS							
Combinatorial delay F/G inputs to X/Y outputs	T_{ILO}	See figures 4 and 5, as applicable.	6/	01		3.9	ns
Combinatorial delay F/G inputs via H' to X/Y outputs	T_{IHO}		6/			5.9	
Combinatorial delay C inputs via H' to X/Y outputs	T_{HHO}		6/			4.9	
CLB fast carry logic operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		7/			4.4	
CLB fast carry logic add/ subtract input (F3) to C_{OUT}	T_{ASCY}		7/			6.8	
CLB fast carry logic initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		7/			2.9	
CLB fast carry logic C_{IN} through function generators to X/Y outputs	T_{SUM}		7/			5	
CLB fast carry logic C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		7/			1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLB SWITCHING CHARACTERISTICS - Continued.							
Sequential delays clock K to outputs Q	T_{CKO}	See figures 4 and 5, as applicable	6/			15	ns
Set-up time before clock K, F/G inputs	T_{ICK}		6/		4		
Set-up time before clock K, F/G inputs via H'	T_{IHCK}		6/		6.1		
Set-up time before clock K, C inputs via H1	T_{HHCK}		6/		5		
Set-up time before clock K, C inputs via DIN	T_{DICK}		6/		3		
Set-up time before clock K, C inputs via EC	T_{ECCK}		6/		4		
Set-up time before clock K, C inputs via S/R, going low (inactive)	T_{RCK}		3/		4.2		
Hold time after clock K, F/G inputs	T_{CKI}		6/		0		
Hold time after clock K, F/G inputs via H'	T_{CKIH}		6/		0		
Hold time after clock K, C inputs via H1	T_{CKHH}		6/		0		
Hold time after clock K, C inputs via DIN	T_{CKDI}		6/		0		
Hold time after clock K, C inputs via EC	T_{CKEC}		6/		0		
Hold time after clock K, C inputs via S/R, going low (inactive)	T_{CKR}		3/		0		
Clock high time	T_{CH}		3/		4.5		
Clock low time	T_{CL}		3/		4.5		
Set/Reset direct width (high)	T_{RPW}		3/		5.5		
Set/Reset direct delay, from C to Q	T_{RIO}		6/			6.5	
Master set/reset width (high or low)	T_{MRW}		3/		13		
Master set/reset delay from global set/reset net to Q	T_{MRQ}		3/			23	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLB SWITCHING CHARACTERISTICS (RAM OPTION)							
Read operation, address read cycle time (16 X 2)	T_{RC}	See figures 3 and 4, as applicable. 7/	4/	01	4.5		ns
Read operation, address read cycle time (32 X 1)	T_{RCT}		4/		6.5		
Read operation data valid after address change (no write enable) (16 X 2)	T_{ILO}		4/			3.9	
Read operation data valid after address change (no write enable) (32 X 1)	T_{IHO}		4/			5.9	
Read during write, clocking data into flip flop address setup time before clock K (16 X 2)	T_{ICK}		4/		4		
Read during write, clocking data into flip flop address setup time before clock K (32 X 1)	T_{IHCK}		4/		6.1		
Read during write, data valid after WE going active (16 X 2)	T_{WO}		4/			10	
Read during write, (DIN stable before WE) (32 X 1)	T_{WOT}		4/			12	
Read during write, data valid after DIN (16 X 2)	T_{DO}		4/			9	
Read during write, (DIN change during WE) (32 X 1)	T_{DOT}		4/			11	
Read during write, clocking data into flip flop, WE setup time before clock K (16 X 2)	T_{WCK}		4/		8		
Read during write, clocking data into flip flop, WE setup time before clock K (32 X 1)	T_{WCKT}		4/		9.6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLB SWITCHING CHARACTERISTICS (RAM OPTION) - Continued.							
Read during write, clocking data into flip flop, data setup time before clock K (16 X 2)	T_{DCK}	See figures 3 and 4, as applicable. 7/	4/		7		ns
Read during write, clocking data into flip flop, data setup time before clock K (32 X 1)	T_{DCKT}		4/		8		
Write operation, address write cycle time (16 X 2)	T_{WC}		4/		8		
Write operation, address write cycle time (32 X 1)	T_{WCT}		4/		8		
Write operation, write enable pulse width (high) (16 X 2)	T_{WP}		4/		4		
Write operation, write enable pulse width (high) (32 X 1)	T_{WPT}		4/		4		
Write operation, address setup time before beginning of WE (16 X 2)	T_{AS}		4/		2		
Write operation, address setup time before beginning of WE (32 X 1)	T_{AST}		4/		2		
Write operation, address hold time after end of WE (16 X 2)	T_{AH}		4/		2		
Write operation, address hold time after end of WE (32 X 1)	T_{AHT}		4/		2		
Write operation, DIN setup time before end of WE (16 X 2)	T_{DS}		4/		4		
Write operation, DIN setup time before end of WE (32 X 1)	T_{DST}		4/		5		
Write operation, DIN hold time after end of WE	T_{DHT}		4/		2		

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
IOB SWITCHING CHARACTERISTICS							
Input propagation delay, pad to I1, I2	T_{PID}	See figures 3 and 4 as applicable. 9/ 10/	5/	01		3	ns
Input propagation delay, pad to I1, I2, via transparent latch (fast)	T_{PLI}		4/			6	
Input propagation delay, pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		4/			12	
Input propagation delay, clock (IK) to I1, I2, (flip-flop)	T_{IKRI}		4/			6.8	
Input propagation delay, clock (IK) to I1, I2, (latch enable)	T_{IKLI}		4/			7.3	
Setup time, pad to clock (IK), fast	T_{PICK}	See figures 3 and 4 as applicable. 10/ 11/ 12/	4/		4		
Setup time, pad to clock (IK), with delay	T_{PICKD}		4/		10.9		
Hold time, pad to clock (IK), fast	T_{IKPI}		4/		0		
Hold time, pad to clock (IK), with delay	T_{IKPID}		4/		0		
Output propagation delay clock (OK) to pad, (fast)	T_{OKPOF}	See figures 3 and 4 as applicable. 9/ 10/	4/			7.5	
Output propagation delay clock (OK) to pad, (slew rate limited)	T_{OKPOS}		4/			11.5	
Output propagation delay output (O) to pad (fast)	T_{OPF}		4/			8	

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
IOB SWITCHING CHARACTERISTICS - continued							
Output propagation delay output (O) to pad (slew rate limited)	T_{OPS}	See figures 3 and 4 as applicable. 9/ 10/	5/	01		12	ns
Output propagation delay 3-state to pad begin hi-Z (fast)	T_{TSHZF}		8/			10	
Output propagation delay 3-state to pad active and valid (fast)	T_{TSONF}		8/			10	
Output propagation delay 3-state to pad active and valid (slew rate limited)	T_{TSONS}		8/			13.7	
Setup time, output (O) to clock (OK)	T_{OOK}		4/		5		
Hold time, output (O) to clock (OK)	T_{OKO}		4/		0		
Clock high or low time	T_{CH}/ T_{CL}		4/		4.5		
Global set/reset delay from GSR net through Q to I1, I2	T_{RRI}		4/			12	
Global set/reset delay from GSR net to pad	T_{RPO}		4/			15	
Global set/reset GSR width	T_{MRW}		4/		13		

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified			Group A subgroups	Device types	Limits		Unit
							Min	Max	
GUARANTEED INPUT AND OUTPUT PARAMETERS (Pin to Pin, TTL inputs)									
Global clock to output (fast) using OFF	T_{ICKOF}	OFF = Output Flip-Flop; IFF = Input Flip-Flop or Latch			11/	01		14	ns
Global clock to output (slew-limited) using OFF	T_{ICKO}							18	
Input setup time, using IFF (no delay)	T_{PSUF}						2		
Input hold time, using IFF (no delay)	T_{PHF}						4.6		
Input setup time, using IFF (with delay)	T_{PSU}						8.5		
Input hold time, using IFF (with delay)	T_{PH}						0		
CLB EDGE TRIGGERED (Synchronous) RAM SWITCHING CHARACTERISTICS GUIDELINES									
Address write cycle time (clock K period)	T_{WCS}	See figure 5	→ Size of RAM →	16x2	4/ 13/	01	15		ns
	T_{WCTS}			32X1			15		
Clock K pulse width (active edge)	T_{WPS}			16X2			7.5		
								1	ms
	T_{WPTS}			32X1			7.5		ns
								1	ms
Address setup time before clock K	T_{ASS}			16X2			2.8		ns
	T_{ASTS}			32X1			2.8		
Address hold time after clock K	T_{AHS}			16X2			0		
	T_{AHTS}			32X1			0		
DIN setup time before clock K	T_{DSS}			16X2			3.5		
	T_{DSTS}			32X1			2.5		
DIN hold time after clock K	T_{DHS}			16X2			0		
	T_{DHTS}			32X1			0		

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified			Group A subgroups	Device types	Limits		Unit
							Min	Max	
CLB EDGE TRIGGERED (Synchronous) RAM SWITCHING CHARACTERISTICS GUIDELINES -Continued									
WE setup time before clock K	T_{WSS}	See figure 5	→ Size of RAM →	16X2	12/ 13/	01	2.2		ns
	T_{WSTS}			32X1			2.2		
WE hold time after clock K	T_{WHS}			16X2			0		
	T_{WHTS}			32X1			0		
Data valid after clock K	T_{WOS}			16X2				10.3	
	T_{WOTS}			32X1				11.6	
CLB EDGE TRIGGERED (Synchronous) DUAL-PORT RAM SWITCHING CHARACTERISTICS GUIDELINES									
Address write cycle time (clock K period)	T_{WCDS}	See figure 6	→ Size of RAM →	16X1	12/ 13/	01	15		ns
Clock K pulse width (active edge)	T_{WPDS}			16X1			7.5		
								1	ms
Address setup time before clock K	T_{ASDS}			16X1			2.8		ns
Address hold time after clock K	T_{AHDS}			16X1			0		
DIN setup time before clock K	T_{DSDS}			16X1			2.2		
Din hold time after clock K	T_{DHDS}			16X1			0		
WE setup time before clock K	T_{WSDS}			16X1			2.2		
WE hold time after clock K	T_{WHDS}			16X1			0.3		
Data valid after clock K	T_{WODS}			16X1				10	

1/ With 50 percent of the outputs simultaneously sinking 4 mA.

2/ With no output current loads, no active input or long line pull-resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits "tie" option.

3/ These delays are specified from the decoder input to the decoder output. For pad-to-pad delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}).

TABLE I. Electrical Performance Characteristics - continued.

4/ Parameter is not tested but is guaranteed by characterization data which is taken at initial device introduction and prior to the introduction of significant changes.

5/ Parameter is not directly tested. Devices are first 100 percent functionality tested. Benchmark patterns (t_{B1} - t_{B13}) are then used to determine the compliance of this parameter. Characterization data is taken at initial device introduction and prior to the introduction of significant changes.

6/ Benchmark patterns (t_{B1} - t_{B13}) are used to determine compliance to this parameter.

7/ Timing for the 16 X 1 RAM option is identical to 16 X 2 RAM timing.

8/ Values indicated are guaranteed by characterization data if application note, provided by manufacturer, is followed. If application note is not followed, indicated values are typical only.

9/ Timing is measured at pin threshold, with 50 pF external capacitive loads including test fixture. Slew rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew rate limited outputs this total is two times larger. Exceeding this maximum capacitive load can result in ground bounce of greater than 1.5 V amplitude, less than 5 ns duration, which might cause problems when the LCA drives clocks and other asynchronous signals.

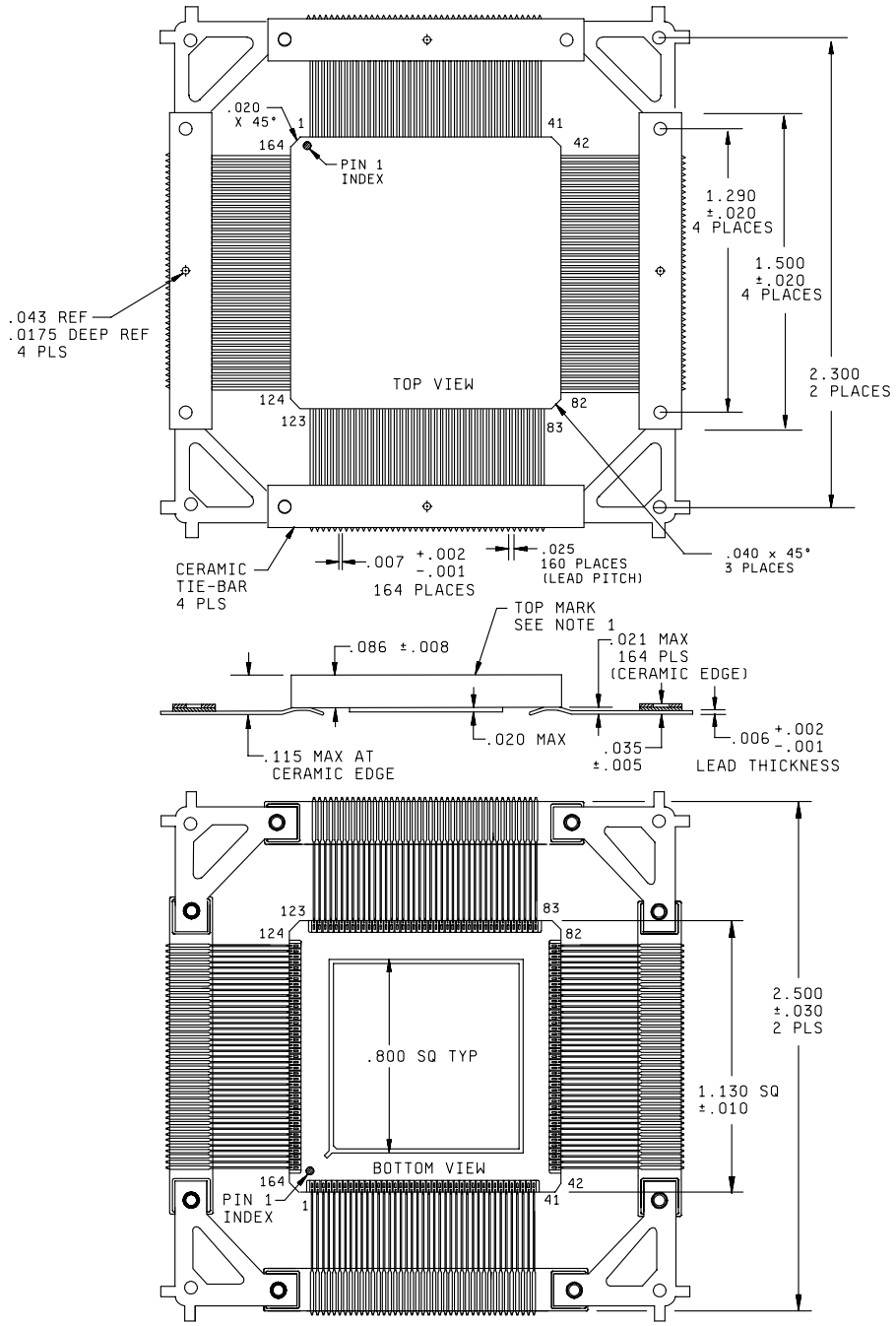
10/ Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

11/ Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. "Negative" hold time means that the delay in the input data is adequate for the external system hold time to be zero, provided the input clock uses the global signal distribution from pad to IK.

12/ Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Some internal timing parameters are derived from benchmark timing patterns.

13/ Timing for the 16X1 RAM option is identical to 16X2 RAM timing. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Case Y

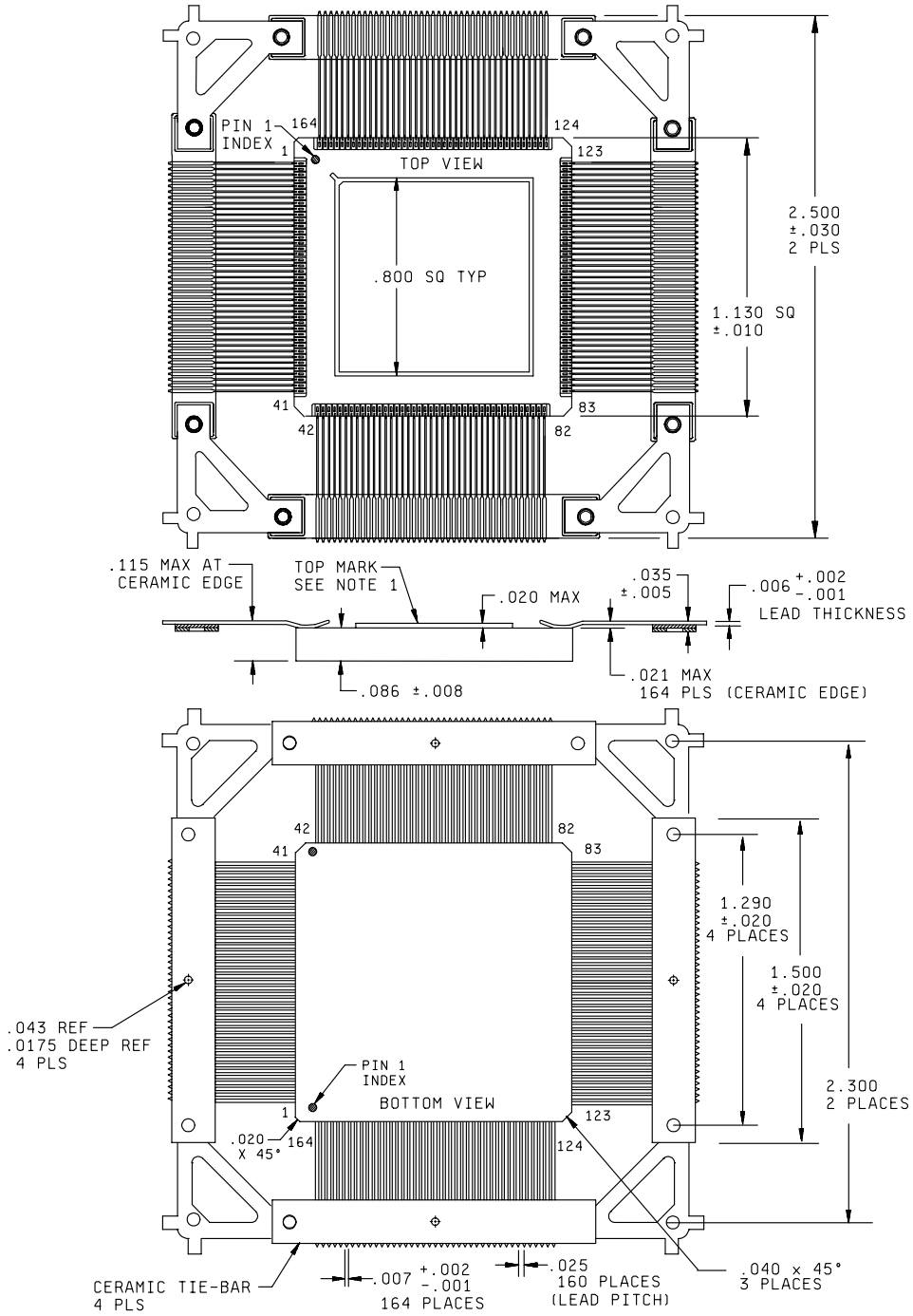


NOTE:

1. Package has top marking on lid side, therefore, pin out goes counterclockwise when device is mounted with lid in up position. (See additional notes on page 18)

FIGURE 1. Case outline.

Case Z



NOTE:

1. Package has top marking on non-lid side, therefore, pin out goes clockwise when device is mounted with lid in down position. (See additional notes on page 18)

FIGURE 1. Case outline - Continued.

Inches	mm		Inches	mm
.001	0.02		.035	0.89
.002	0.05		.040	1.02
.005	0.13		.043	1.09
.006	0.15		.086	2.18
.007	0.18		.115	2.92
.008	0.20		.695	17.65
.010	0.25		.800	20.32
.0175	0.44		.845	21.46
.020	0.51		1.130	28.70
.021	0.53		1.290	32.77
.025	0.64		1.500	38.10
.030	0.76		2.300	58.42
			2.500	63.50

NOTES:

The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.

Case outline X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	I/O (A17)		C1	I/O (A13)		F15	I/O
A2	I/O		C2	I/O		F16	I/O
A3	I/O (TCK)		C3	V_{CC}		G1	I/O (A9)
A4	NC		C4	GND		G2	I/O
A5	I/O (TMS)		C5	I/O		G3	I/O
A6	I/O		C6	GND		G14	I/O
A7	I/O		C7	I/O		G15	I/O
A8	I/O		C8	GND		G16	I/O
A9	I/O		C9	I/O		H1	I/O (A8)
A10	I/O		C10	I/O		H2	GND
A11	I/O		C11	GND		H3	V_{CC}
A12	NC		C12	I/O		H14	V_{CC}
A13	I/O		C13	GND		H15	I/O ($\overline{ERR}$, $\overline{INIT}$)
A14	I/O		C14	V_{CC}		H16	I/O
A15	M1		C15	I/O		J1	I/O
A16	M0		C16	I/O (LDC)		J2	I/O (A6)
B1	I/O (A14)		D1	NC		J3	I/O (A7)
B2	SGCK1 (A15, I/O)		D2	NC		J14	GND
B3	PGCK1 (A16, I/O)		D3	I/O		J15	I/O
B4	I/O (TDI)		D14	I/O (HDC)		J16	I/O
B5	I/O		D15	I/O			
B6	I/O		D16	NC			
B7	I/O		E1	I/O			
B8	V_{CC}		E2	I/O			
B9	I/O		E3	I/O (A12)			
B10	I/O		E14	I/O			
B11	I/O		E15	NC			
B12	I/O		E16	I/O			
B13	I/O		F1	I/O (A10)			
B14	SGCK2 (I/O)		F2	I/O (A11)			
B15	M2		F3	GND			
B16	PGCK2 (I/O)		F14	GND			

NC = NO CONNECT

FIGURE 2. Terminal connections.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
K1	I/O		P11	GND		T13	I/O
K2	I/O (A5)		P12	I/O		T14	I/O (D6)
K3	I/O (A4)		P13	V_{CC}		T15	PGCK3 (I/O)
K14	I/O		P14	GND		T16	I/O (D7)
K15	I/O		P15	I/O			
K16	I/O		P16	I/O			
L1	I/O		R1	I/O (A0, $\overline{WS}$)			
L2	I/O		R2	CCLK			
L3	GND		R3	I/O			
L14	GND		R4	I/O			
L15	I/O		R5	NC			
L16	I/O		R6	I/O			
M1	NC		R7	I/O			
M2	NC		R8	V_{CC}			
M3	I/O		R9	I/O (D4)			
M14	I/O		R10	I/O			
M15	NC		R11	I/O			
M16	I/O		R12	NC			
N1	I/O (A3)		R13	I/O			
N2	I/O		R14	$\overline{PROG}$			
N3	GND		R15	DONE			
N14	I/O		R16	SGCK3 (I/O)			
N15	I/O		T1	TD0			
N16	NC		T2	SGCK4 (DOUT, I/O)			
P1	I/O ($\overline{CS1}$, A2)		T3	I/O (D1)			
P2	PGCK4 (A1, I/O)		T4	I/O			
P3	V_{CC}		T5	I/O			
P4	I/O (D0, DIN)		T6	I/O			
P5	I/O ($\overline{RCLK}$ - $\overline{BUSY}$ /RDY)		T7	I/O ($\overline{RS}$)			
P6	GND		T8	I/O (D3)			
P7	I/O (D2)		T9	I/O			
P8	GND		T10	I/O (D5)			
P9	I/O		T11	I/O			
P10	I/0 ($\overline{CS0}$)		T12	NC			

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

Case outline Y and Z

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	GND		29	I/O		57	I/O
2	PGCK1 (A16, I/O)		30	GND		58	I/O
3	I/O (A17)		31	NC		59	I/O
4	I/O		32	I/O		60	I/O
5	I/O		33	I/O		61	I/O ($\overline{ERR}$, $\overline{INIT}$)
6	NC		34	I/O		62	V_{CC}
7	I/O (TDI)		35	I/O		63	GND
8	I/O (TCK)		36	NC		64	I/O
9	NC		37	I/O		65	I/O
10	GND		38	SGCK2 (I/O)		66	I/O
11	I/O		39	M1		67	I/O
12	I/O		40	GND		68	I/O
13	I/O (TMS)		41	M0		69	I/O
14	I/O		42	V_{CC}		70	I/O
15	I/O		43	M2		71	I/O
16	I/O		44	PGCK2 (I/O)		72	GND
17	I/O		45	I/O (HDC)		73	NC
18	I/O		46	I/O		74	NC
19	GND		47	NC		75	I/O
20	V_{CC}		48	I/O		76	I/O
21	I/O		49	I/O		77	I/O
22	I/O		50	I/O (LDC)		78	I/O
23	I/O		51	NC		79	I/O
24	I/O		52	NC		80	SGCK3 (I/O)
25	NC		53	GND		81	GND
26	I/O		54	I/O		82	DONE
27	I/O		55	I/O		83	V_{CC}
28	I/O		56	I/O		84	$\overline{PROG}$

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
85	I/O (D7)		112	I/O		139	I/O (A5)
86	PGCK3 (I/O)		113	GND		140	I/O
87	I/O		114	NC		141	I/O
88	NC		115	I/O (D1)		142	I/O (A6)
89	I/O		116	I/O ($\overline{\text{RCLK}}$ - $\overline{\text{BUSY}}$ /RDY)		143	I/O (A7)
90	I/O (D6)		117	I/O		144	GND
91	I/O		118	NC		145	V_{CC}
92	NC		119	I/O		146	I/O (A8)
93	NC		120	I/O (D0, DIN)		147	I/O (A9)
94	GND		121	SGCK4 (DOUT,I/O)		148	I/O
95	I/O		122	CCLK		149	I/O
96	I/O		123	V_{CC}		150	I/O (A10)
97	I/O (D5)		124	TDO		151	I/O (A11)
98	I/O ($\overline{\text{CS0}}$)		125	GND		152	I/O
99	I/O		126	I/O (A0, $\overline{\text{WS}}$)		153	I/O
100	I/O		127	PGCK4, (A1, I/O)		154	GND
101	I/O (D4)		128	I/O		155	NC
102	I/O		129	NC		156	NC
103	V_{CC}		130	I/O		157	I/O (A12)
104	GND		131	I/O ($\overline{\text{CS1}}$, A2)		158	I/O (A13)
105	I/O (D3)		132	I/O (A3)		159	NC
106	I/O ($\overline{\text{RS}}$)		133	NC		160	I/O
107	I/O		134	NC		161	I/O
108	I/O		135	GND		162	I/O (A14)
109	I/O (D2)		136	I/O		163	SGCK1 (A15, I/O)
110	I/O		137	I/O		164	V_{CC}
111	I/O		138	I/O (A4)			

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

I/O BLOCK

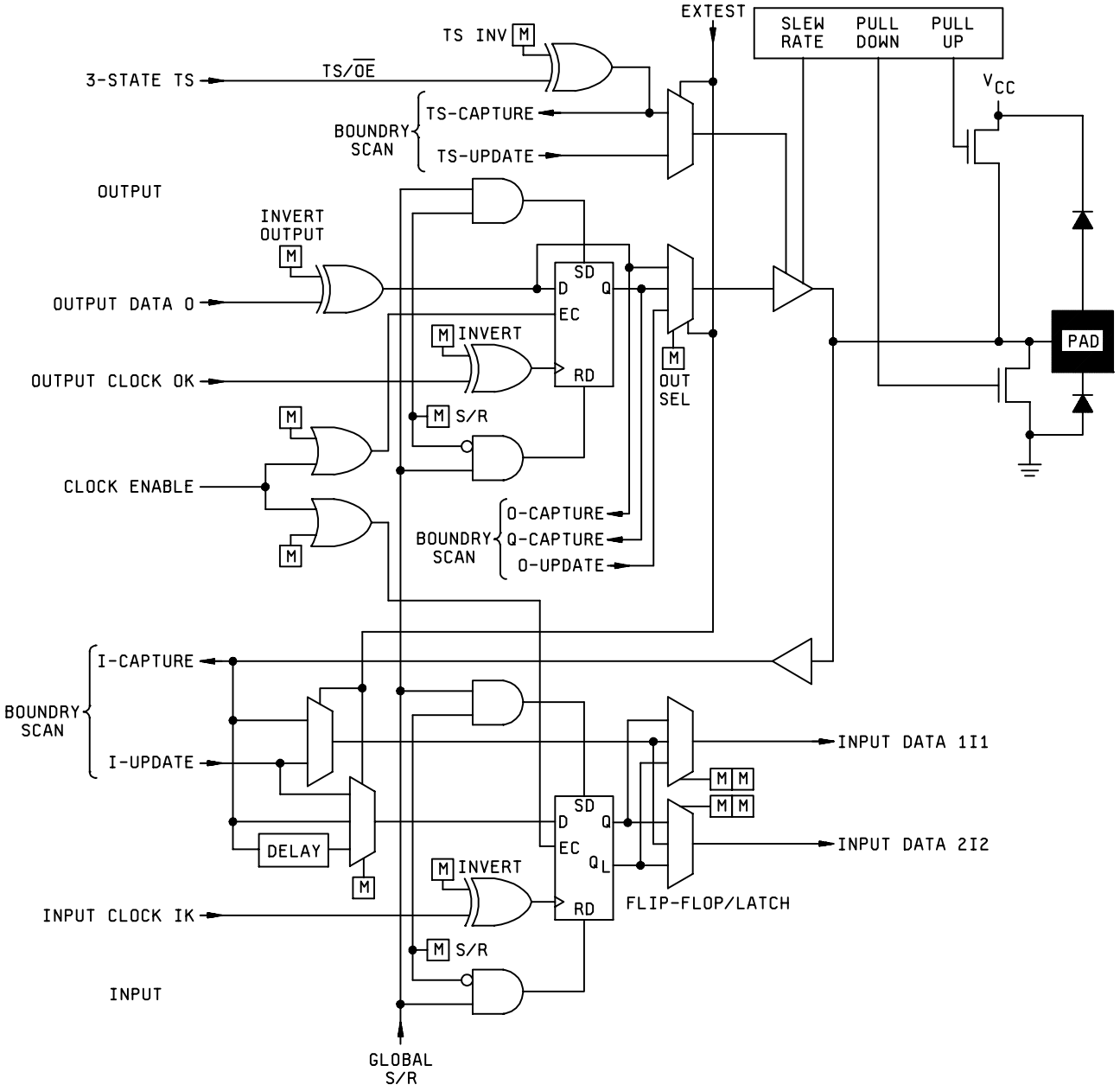
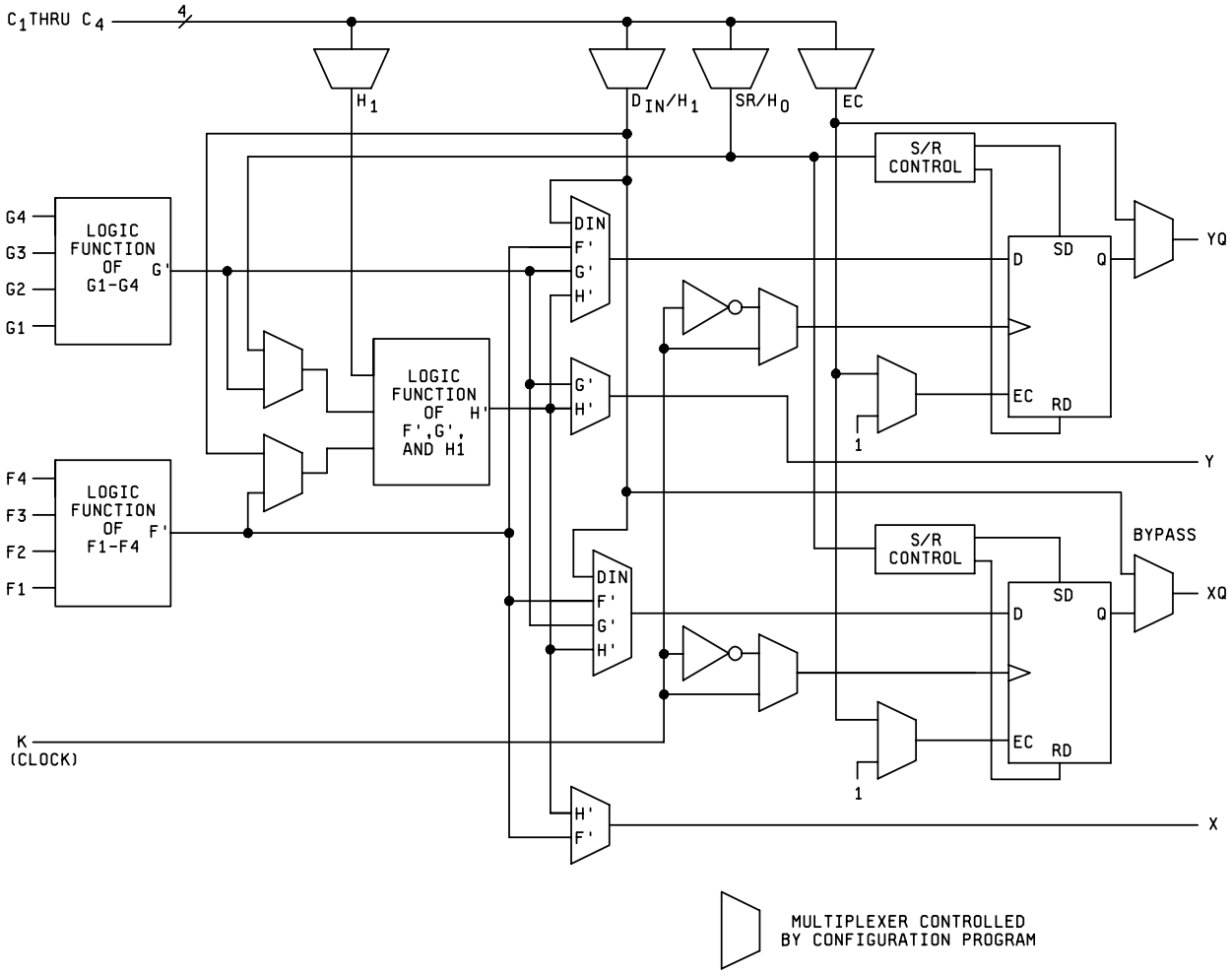


FIGURE 3. Logic block diagrams.

Simplified block diagram of CLB



(RAM and Carry logic functions not shown)

FIGURE 3. Logic block diagrams - Continued.

CONFIGURABLE LOGIC BLOCK (CLB)

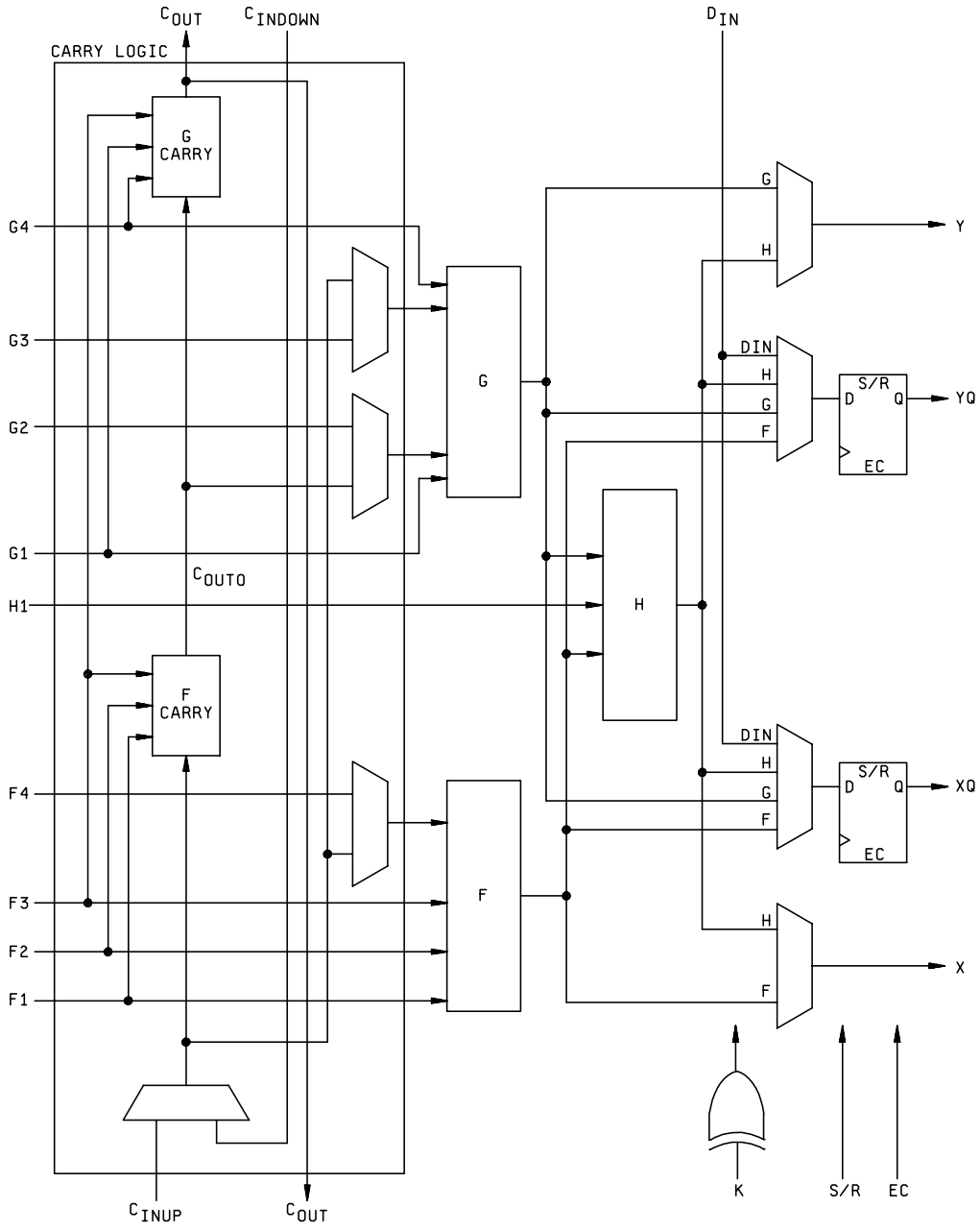


FIGURE 3. Logic block diagrams - Continued.

Detail of dedicated carry logic

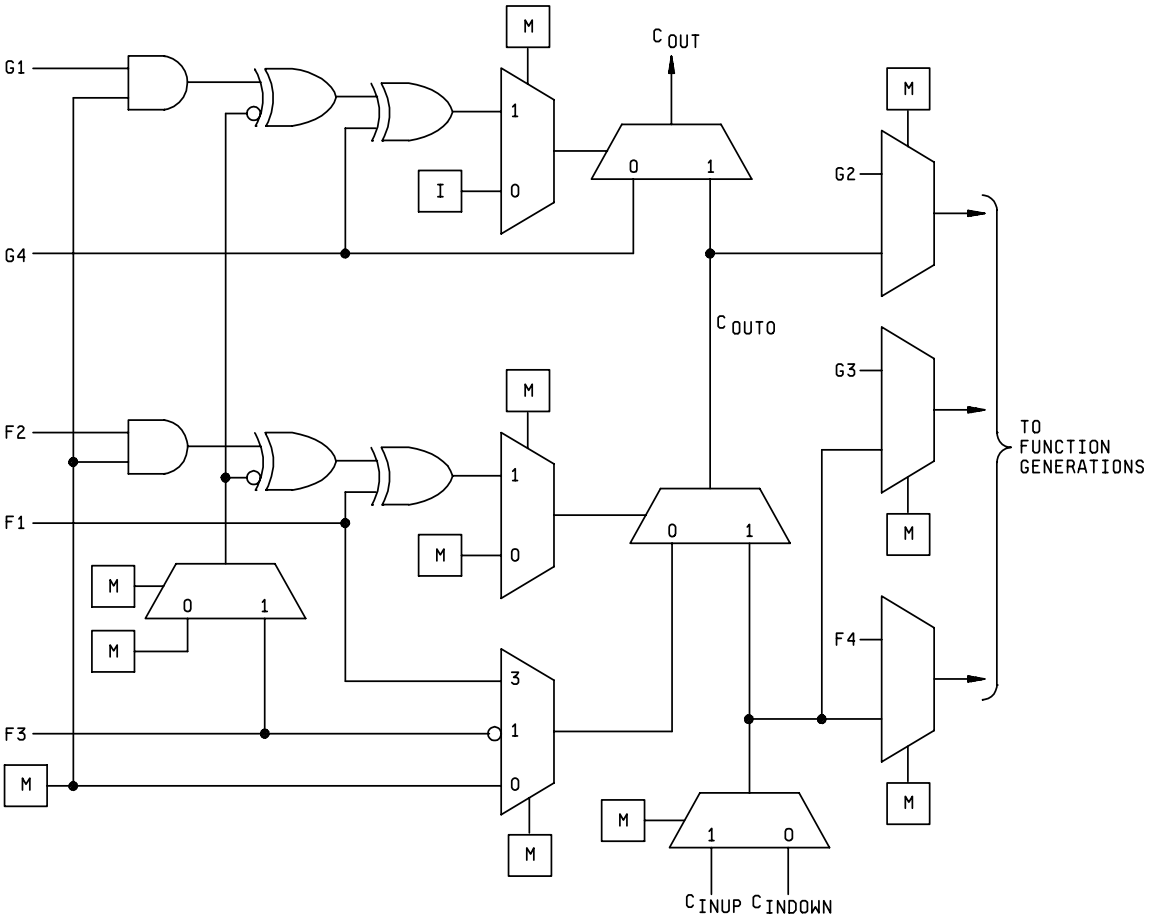
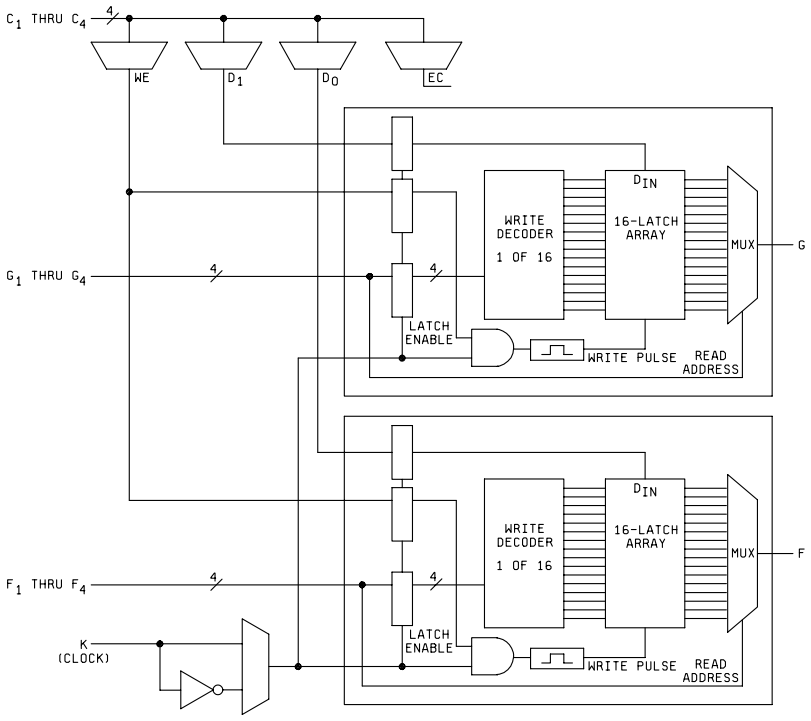


FIGURE 3. Logic block diagrams - Continued.



16 X 2 (or 16 X 1) edge-triggered single port RAM

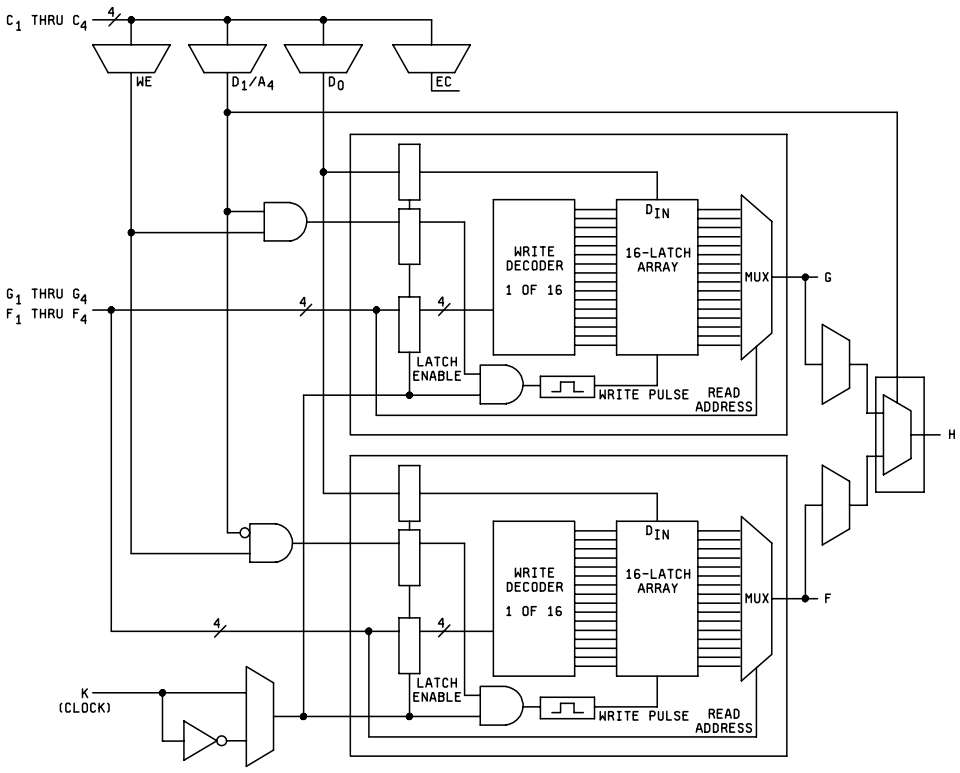


FIGURE 3. Logic block diagrams - Continued.

16 X 1 edge-triggered dual-port RAM

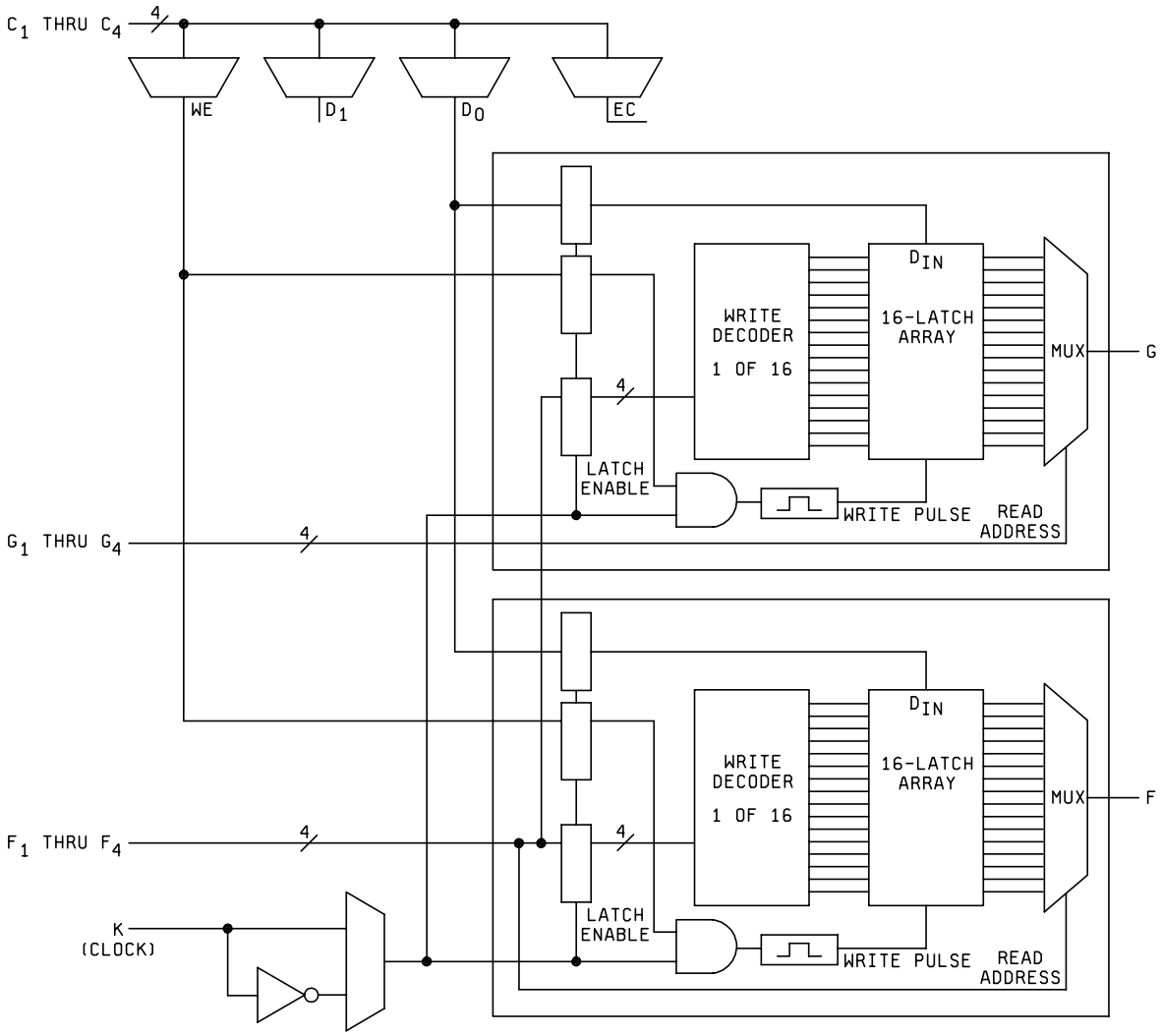


FIGURE 3. Logic block diagrams - Continued.

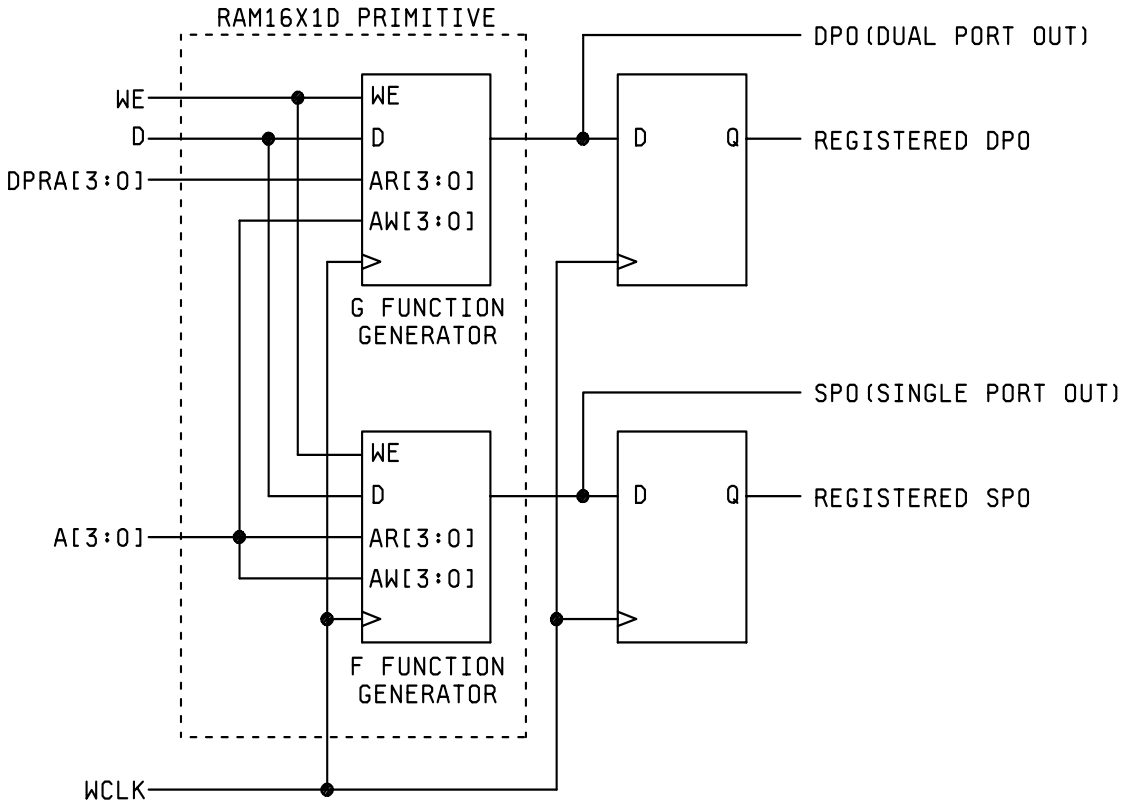


FIGURE 3. Logic block diagrams - Continued.

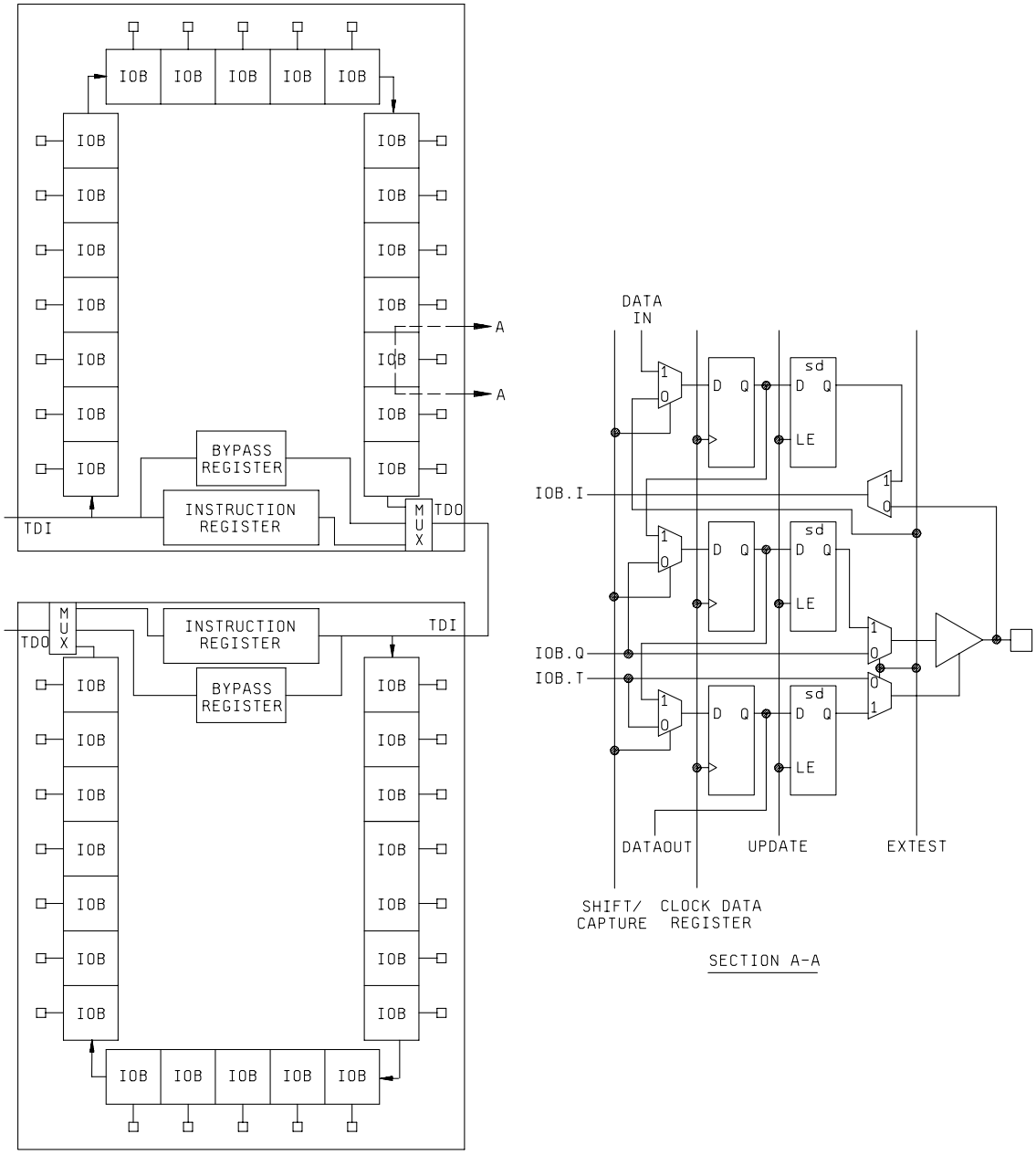


FIGURE 3. Logic block diagrams - Continued.

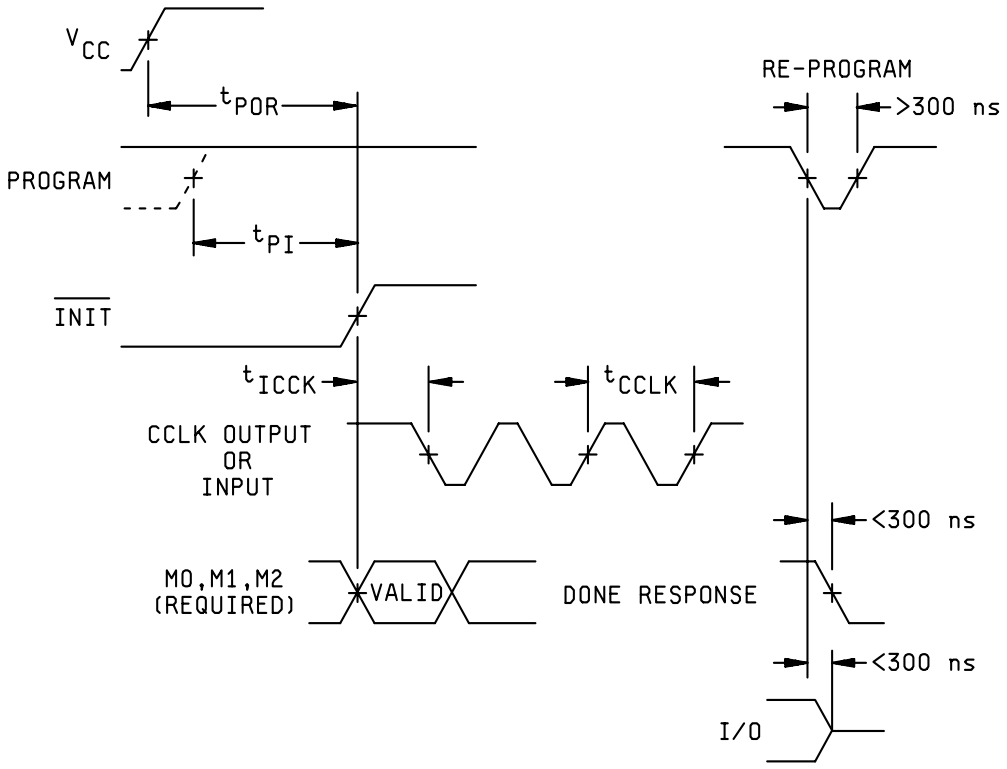


FIGURE 4. Timing diagrams and switching characteristics.

CONFIGURABLE LOGIC BLOCK (CLB) SWITCHING CHARACTERISTICS

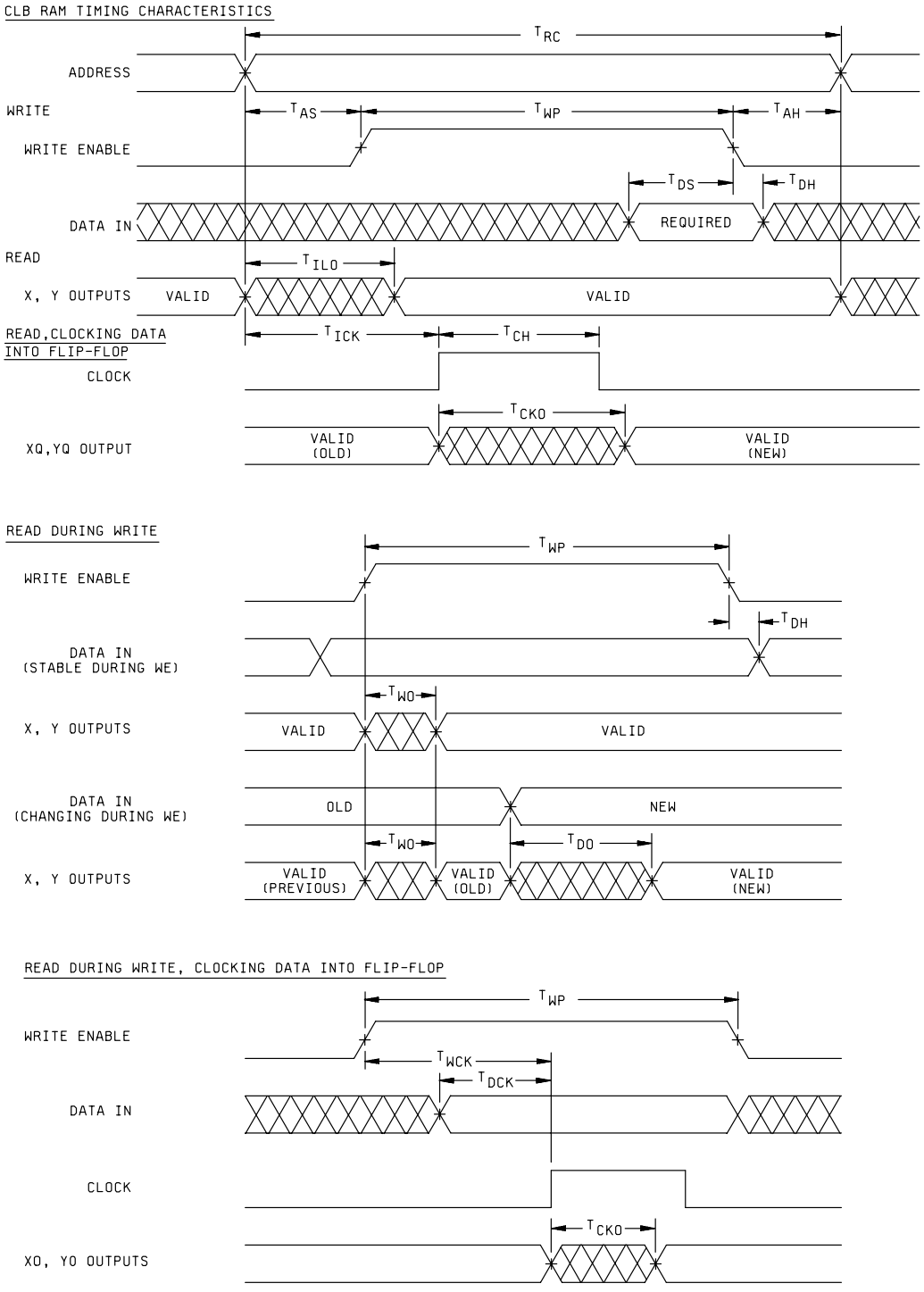


FIGURE 4. Timing diagrams and switching characteristics - Continued.

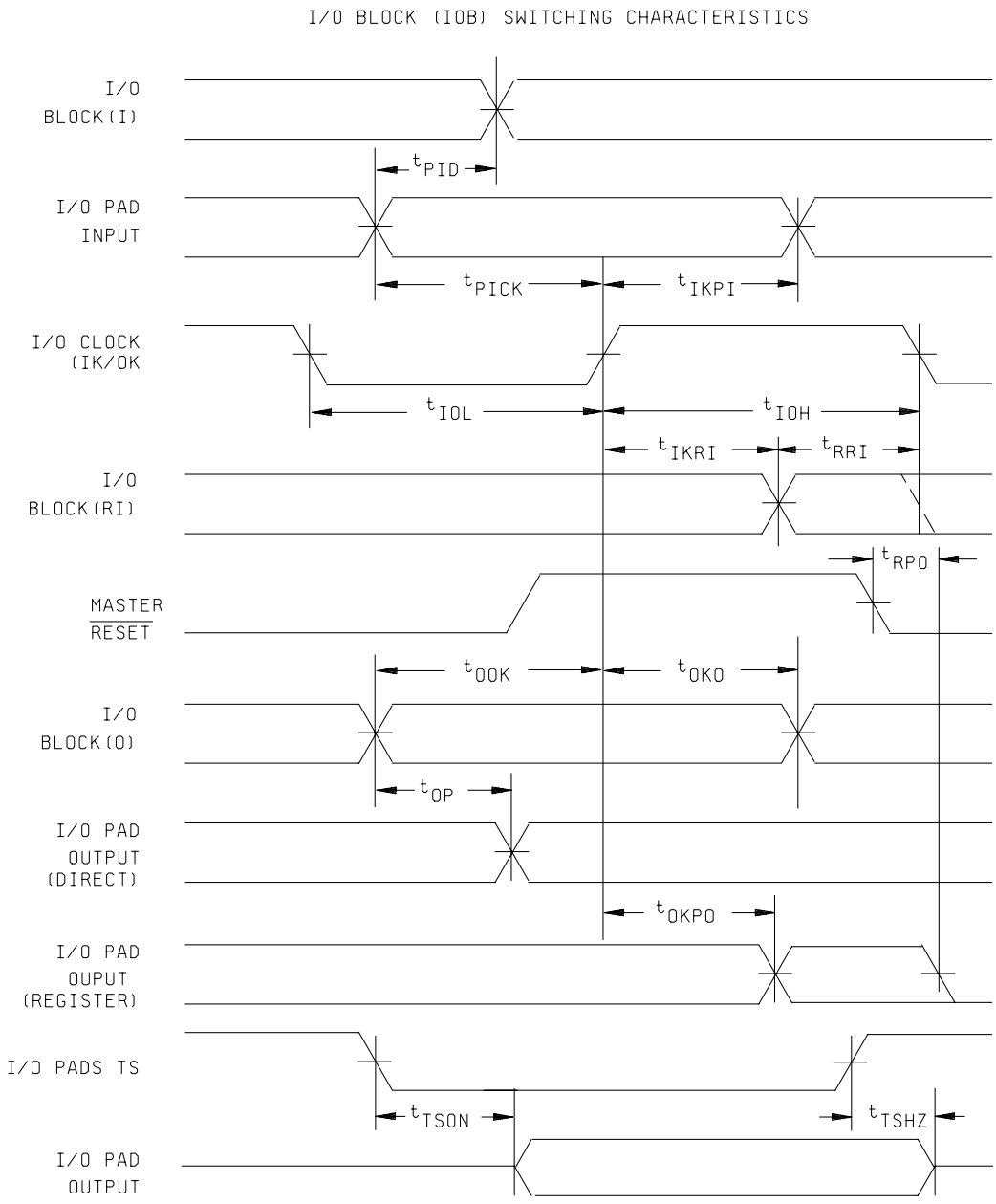
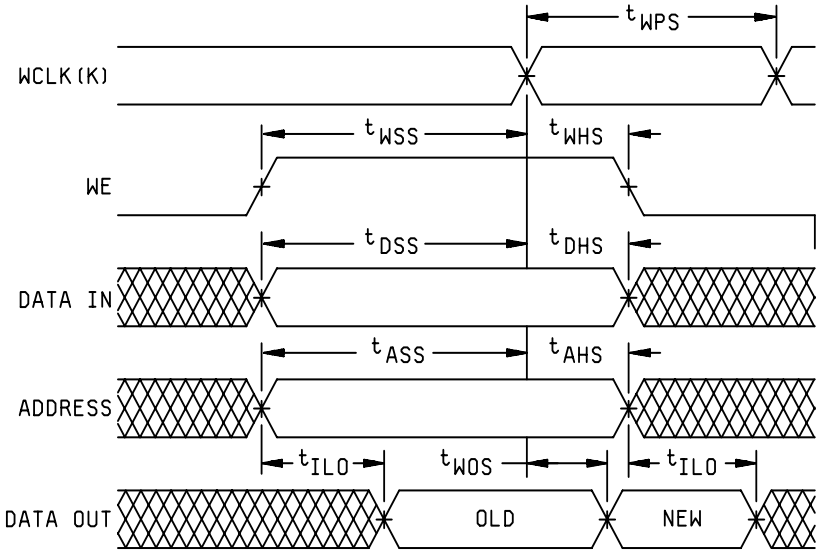


FIGURE 4. Timing diagrams and switching characteristics - Continued.

SYNCHRONOUS DRAM



DUAL PORT RAM

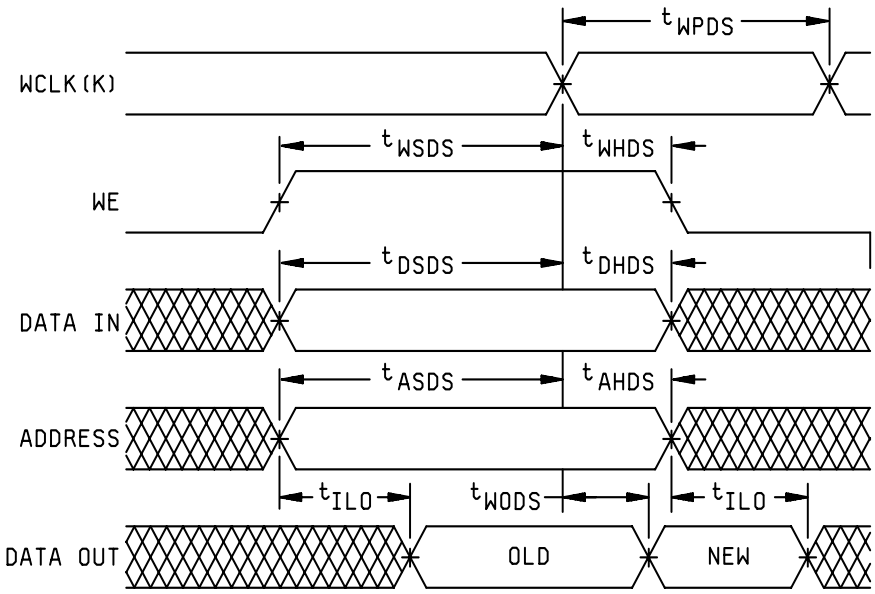
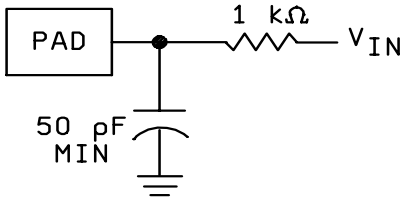
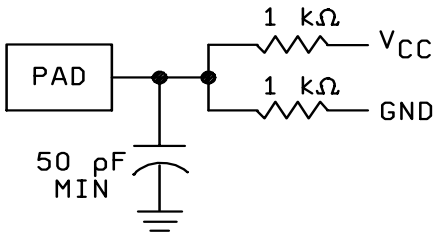


FIGURE 4. Timing diagrams and switching characteristics - Continued.



CIRCUIT A



CIRCUIT B

FIGURE 5. Load circuit.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall include verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 3 devices with no failures, and all input terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1* Δ
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Not Required
5	Final electrical parameters (see 4.2)	1*, 2, 3,7*, 8A,8B,9,10,11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
6	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCO} standby	±1 mA of specified limit in table I.
I_{IL}	±1 µA of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

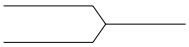
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

V_{CC}	+5.0 V SUPPLY VOLTAGE
GND	GROUND
CCLK	CONFIGURATION CLOCK
DONE	DONE
PROGRAM	PROGRAM
RCLK	READ CLOCK
M0	MODE 0
M1	MODE 1
M2	MODE 2
TDO	TEST DATA OUTPUT
TDI	TEST DATA IN
TCK	TEST CLOCK
TMS	TEST MODE SELECT
HDC	HIGH DURING CONFIGURATION
LDC	LOW DURING CONFIGURATION
INIT	INIT
PGCK1-PGCK4	PRIMARY GLOBAL INPUTS
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.
CSO	CHIP SELECT, WRITE
CS1	CHIP SELECT, WRITE
WS	WRITE STROBE
RS	READ STROBE
A0-A17	ADDRESS
D0-D7	DATA
DIN	DATA INPUT
DOUT	DATA OUTPUT
I/O	INPUT/OUTPUT

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

BUFFER SWITCHING CHARACTERISTICS

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TBUF driving a horizontal Longline (L.L.) I to L.L. while T is low (buffer active)	T_{IO1}	See note.	N/A	All		5.0	ns
TBUF driving a horizontal Longline (L.L.) I going low to L.L. going from resistive pull up high to active low, (TBUF configured as open drain	T_{IO2}					6.0	
T going low to L.L. active and valid	T_{ON}					7.0	
T to L.L. inactive	T_{OFF}					1.8	
T going high to L.L. (inactive) with single pull-up resistor	T_{PUS}					23	
T going high to L.L. (inactive) with pair of pull-up resistor	T_{PUF}					10	

NOTE: These values are typical. They are not tested, characterized, or guaranteed but are derived from benchmark timing patterns.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-05-10

Approved sources of supply for SMD 5962-97522 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9752201QXC	68994	XC4005E-4PG156B
5962-9752201QYC	68994	XC4005E-4B164B
5962-9752201QZC	68994	XC4005E-4B164B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124