

XC4000H High I/O Count Logic Cell Array Family

Product Specifications

Features

- Third-generation Field-Programmable Gate Arrays
 - Very high number of I/O pins
 - Abundant flip-flops
 - Flexible function generators
 - On-chip ultra-fast RAM
 - Dedicated high-speed carry-propagation circuit
 - Wide edge decoders (four per edge)
 - Efficient implementation of multi-level logic
 - Hierarchy of interconnect lines
 - Internal 3-state bus capability
 - Eight global low-skew clock or signal distribution network
 - IEEE 1149.1-compatible boundary-scan logic support
 - Programmable output slew rate with (two modes including SoftEdge)
- Per-pin individually configurable input threshold and output high level, either TTL or CMOS
 - Programmable input pull-up or pull-down resistors
- Flexible Array Architecture
 - Programmable logic blocks and I/O blocks
 - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
 - High-speed logic and interconnect
 - Low power consumption
- Configured by Loading Binary File
 - Unlimited reprogrammability
 - Six programming modes
- XACT Development System runs on '386/'486-type PC, NEC PC, Apollo, Sun-4, and Hewlett Packard 700 Series
 - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
 - Fully automatic partitioning, placement and routing
 - Interactive design editor for design optimization
 - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 family provides a regular, flexible, program-

Device	XC4003H	XC4005H
Approximate Gate Count	3,000	5,000
Number of IOBs	160	192
CLB Matrix	10 x 10	14 x 14
Number of CLBs	100	196
Number of Flip-Flops	200	392
Max Decode Inputs (per side)	30	42
Max RAM Bits	3,200	6,272

mable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

The XC4000H family is intended for I/O-intensive applications. Compared to the XC4000, the XC4000H devices have almost double the number of IOBs and I/O pins, and offer a choice of CMOS- or TTL-level outputs and input thresholds, selectable per pin. The XC4000H outputs sink 24 mA and offer improved 3-state and slew-rate control.

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000H family is supported by the same powerful and sophisticated software as the XC4000 family, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally to the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

For a detailed description of the device features, architecture, configuration methods and pin descriptions, see pages 2-9 through 2-45.

XC4000H Compared to XC4000

For readers already familiar with the XC4000 family, here is a concise list of the major new features in the XC4000H family.

- Number of IOBs is, roughly, doubled compared to the XC4000.
- Output slew-rate control is significantly improved.

Resistive Load means a strong pull-down all the way to ground, capable of sinking 24 mA continuously. If many outputs switch simultaneously, the resulting ground bounce might be objectionable.

Capacitive Load, or SoftEdge, means a more sophisticated pull-down that decreases in strength as it approaches ground. It can only sink 4 mA at V_{OL} , which is irrelevant when driving capacitive loads. The benefit is a substantial reduction in ground bounce when several outputs switch simultaneously.

In the XC4000, limiting the slew rate of the output reduces ground bounce, but also introduces a significant additional delay. In the XC4000H, the additional delay in the capacitive-load mode is usually insignificant.

- All input and output flip-flops have been eliminated in the XC4000H family. Use the CLB flip-flops instead.
- Outputs can sink 24 mA, guaranteed at V_{OL} = 0.5 V, compared to the 12 mA at 0.4 V of the XC4000 family.
- Number of decoder inputs per side
- Each output may be individually configured as one of the following.
 - TTL-compatible (like the XC4000) that uses n-channel transistors for both pull-down and pull-up,
 - A totem-pole output structure with reduced V_{OH},
 - CMOS-compatible (like the XC2000 and XC3000) that means n-channel pull-down and p-channel pull-up with V_{OH} close to the V_{CC} rail.
- Each input can individually be configured for either TTLcompatible threshold (1.2 V) or for CMOS-compatible threshold (V_{CC}/2). Each input can be configured to be inverting or non-inverting.
- Any combination of programmable input and output levels on any I/O pin is possible, even the dubious combination of TTL output and CMOS input on the same I/O pin.
- Output 3-state operation is controlled by a two-input multiplexer.
- The first activation of outputs after the end of the configuration process, as they change from 3-state to their active level, is always in the SoftEdge mode. This

prevents potential ground-bounce problems when all outputs turn on simultaneously. A few nanoseconds later, each output assumes the current-sink capability determined by its configuration. This soft wake-up operation is transparent to the user.

Architectural Overview

Except for the I/O structure, the XC4000H family is identical to the original XC4000 family. A matrix of Configurable Logic Blocks is interconnected through a hierarchy of flexible routing resources. The powerful system-integration features of the XC4000 family, such as on-chip RAM, dedicated fast carry, and wide decoders, are retained in the XC4000H family.

The XC4000H family almost doubles the number of input/ output pins compared to the XC4000, an attractive feature for I/O-intensive applications. The output drivers were redesigned to be more powerful and more flexible.

Input/Output Blocks (IOBs)

The IOBs form the interface between the internal logic and the I/O pads of the XC4000H device. Each IOB consists of a programmable output section that can drive the pad, and a programmable input section, that can receive data from the pad. Aside from being connected to the same pad, the input and output sections have nothing else in common.

Input

In XC4000H devices, there are no input flip-flops.

The input section receives data from the pad. Each input can be configured individually with TTL or CMOS input thresholds. As a configuration option, the input can be either inverted or non-inverted, before it is made available to the internal logic.

Pad

Each I/O pad can be configured with or without a pull-up or pull-down resistor, independent of the pin usage.

Boundary Scan

The XC4000H IOBs have the same IEE 1149.1boundaryscan capabilities as the IOBs in the original XC4000.

Output

In an XC4000H IOB, there is no output flip-flop. The output section receives data and 3-state control information from the CLB interconnect structure.

Under configuration control, the data can be inverted or non-inverted. The output driver assumes one of the following states.

- Permanently disabled, making the pad an input only pad
- 3-state controlled from the internal logic

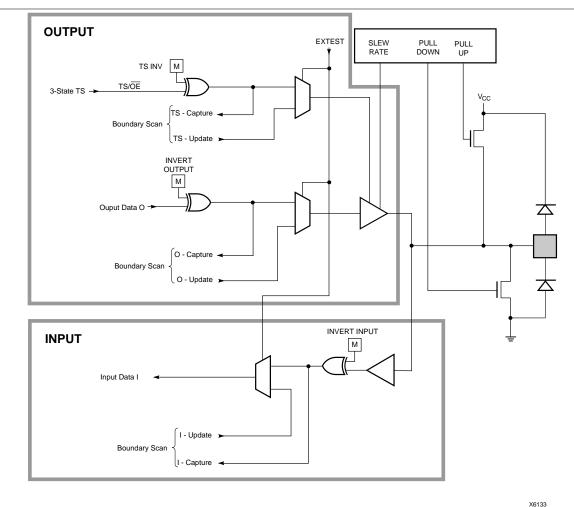
There are two potential sources of the 3-state-control information, selected by a multiplexer. The output of the multiplexer driving the 3-state control can be inverted as a configuration option. The signal can be active High 3-state, which is identical to the more popular connotation of active-Low Output Enable, or it can be active-High Output Enable, which is identical to active Low 3-state.

Each output can be individually configured as either TTLor CMOS-compatible. A TTL-compatible output uses nchannel transistors for both pull-down and pull-up. As a result, the output High voltage, V_{OH} is at least one threshold voltage drop below V_{CC}. Depending on the load current, this means a voltage drop of 1.0 to 2.4 V. In a system using TTL input thresholds of 1.2 V, this lower output voltage results in shorter delays when switching from High to Low, and thus a better delay balance between the two signal directions. The smaller signal amplitude also generates less noise. The reduction in High-level noise margin is irrelevant because it is still much better than the Low-level noise margin. TTL-level outputs are, therefore, the best choice for systems that use TTL-level input thresholds. (XC4000 and XC4000A devices have only TTL-level outputs and have only TTL-level input thresholds).

When the output is configured as CMOS-compatible, an additional p-channel transistor pulls the output towards the V_{CC} rail. This results in an unloaded rail-to-rail signal swing, ideal for systems that use CMOS input thresholds. (XC2000 and XC3000 devices have only CMOS-level outputs).

Each output can be configured for either of two slew-rate options, which affect only the pull-down operation. When configured for resistive load, the pull-down transistor is driven hard, resulting in a practically constant on-resistance of about 10 Ω . This results in the fastest High-to-Low transition, and the capability to sink 24 mA with a voltage of 500 mV. When many outputs switch High to Low simultaneously, especially when they are discharging a capacitive load, this configuration option might result in excessive ground bounce.

When configured for capacitive load, or SoftEdge, the High-to-Low transition starts as described above, but the drive to the pull-down transistor is reduced as soon as the output voltage reaches a value around 1 V. This results in a higher resistance in the pull-down transistor, a slowing down of the falling edge, and a significantly reduced ground bounce.



Slew-Rate Control with SoftEdge

The XC4000H outputs use a novel, patent-pending method of slew-rate control that reduces ground bounce without any significant delay penalty. Each output is configured with a choice between two slew-rate options. Both options reduce the positive ground bounce that occurs when the output current is turned on. They differ in the way the output current is turned off.

• The slew-rate-limited default mode is called capacitive, or SoftEdge. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive until the output voltage has reached +1 V. The pull-down transistor is then gradually turned off, so that it finally has an on-resistance of about 100Ω , low enough to sink 4 mA continuously. Gradually turning off the sink current reduces the max value of current change (di/dt) that is normally responsible for the negative voltage spike over the common ground inductance (bonding wires), called ground bounce.

The capacitive, or SoftEdge, mode is the best choice for capacitively loaded outputs, or for outputs requiring less than 4 mA of dc sink current.

• The non-slew-rate limited mode is called resistive. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive as long as the output data is a logic Low. The pull-down transistor has an impedance of $<20 \Omega$, capable of sinking 24 mA continuously.

Resisitive mode is required for driving terminated transmission lines with 4 to 24 mA of dc sink current. The abrupt current change when the output voltage reaches zero causes a voltage spike over the ground inductance (bonding wire) and can result in objectionable ground bounce when many outputs switch High-to-Low simultaneously. The following figures show output rising and falling edges when one output drives different loads. The tests were performed on a multi-ground-plane test PC board, manufactured by Urban Instruments (Encino, CA). Measurements were done with a Tektronix TDS540 digital storage oscilloscope. The figures below are unedited files from these measurements, the time scale is 2 ns/division.

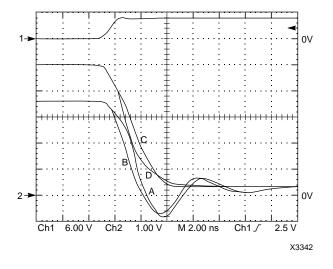
The upper trace in each figure shows a second output driven from the same internal signal, but unloaded. It acts as a timing reference, and triggers the oscilloscope.

Resistive mode and capacitive mode transitions start with practically the same delay from the internal logic. Resisitive mode falls faster, and has more undershoot; capacitive mode rises slightly faster. For a 200- Ω pull-up, 330- Ω pull-down termination, only resisitive mode is meaningful. A TTL-output with a 1000- Ω pull-up, 150-pF termination has a slow (150 ns) final rise time that extends outside the 10-ns timing window of these figures.

Trace A shows Resistive mode with CMOS outputs Trace B shows Resistive mode with TTL outputs Trace C shows Capacitive mode with CMOS outputs Trace D shows Capacitive mode with TTL outputs

Summary

Use resistive mode for applications that require >4 mA of dc sink current, and for heavy capacitive loads when they must be discharged fast. Use capacitive mode for all other applications, especially for light capacitive loads (50 to 200 pF) and for all timing-uncritical outputs that require <4 mA dc current. The Low-to-High transition is not affected by the choice of slew-rate mode.



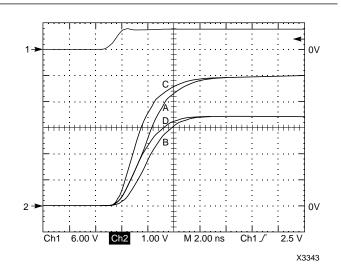


Figure 2. Falling Edge, 50 pF Load



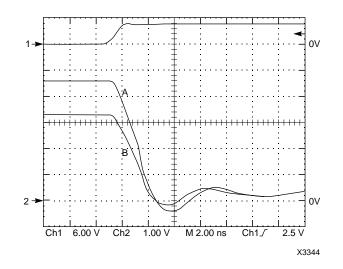


Figure 4. Falling Edge, 200/330 Ω , 50 pF Load

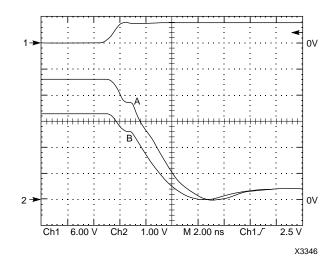


Figure 6. Falling Edge, 200/330 Ω , 150 pF Load

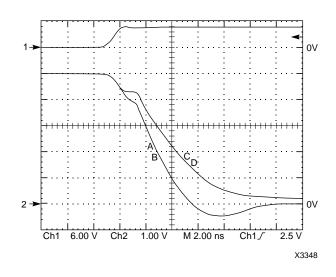


Figure 8. Falling Edge, 1000 Ω , 150 pF Load

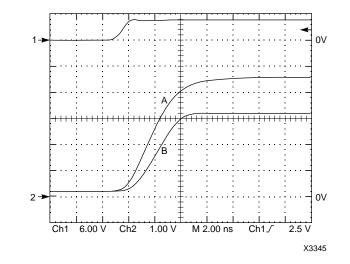


Figure 5. Rising Edge, 200/330 Ω , 50 pF Load

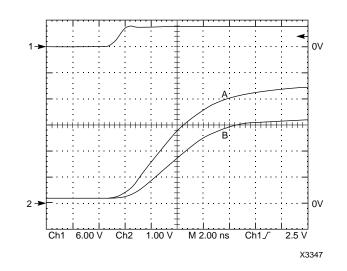
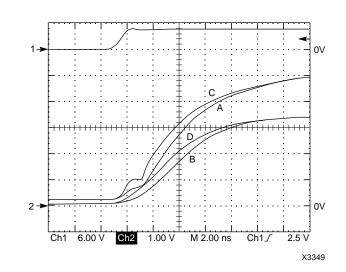


Figure 7. Rising Edge, 200/330 Ω , 150 pF Load





Absolute Maximum Ratings

Symbol	Description		Units
V _{cc}	Supply voltage relative to GND	-0.5 to +7.0	V
V _{IN}	Input voltage with respect to GND	–0.5 to V _{CC} +0.5	V
V _{TS}	Voltage applied to 3-state output	–0.5 to V _{CC} +0.5	V
T _{STG}	Storage temperature (ambient)	–65 to + 150	°C
TJ	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V _{cc}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V _{IH}	High-level input voltage for TTL threshold	2.0	V _{cc}	V
V _{IH}	High-level input voltage for CMOS threshold	70%	100%	V _{cc}
V _{IL}	Low-level input voltage for TTL threshold	0	0.8	V
V _{IL}	Low-level input voltage CMOS threshold	0	20%	V _{cc}

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V _{OH}	High-level output voltage, TTL option @ $I_{OH} = -4.0 \text{ mA}$	2.4		V
V _{OH}	High-level output voltage, CMOS option @ I _{OH} = -1 mA	V _{CC} -0.5		V
V _{OL}	Low-level output voltage @ $I_{OL} = 24$ mA, V_{CC} max (Note 1)		0.5	V
I _{cco}	Quiescent LCA supply current (Note 2)		10	mA
I	Leakage current	-10	+10	μA
C _{IN}	Input capacitance (sample tested)		15	pF
I _{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0V$ (estimate)	0.02	0.20	mA
I _{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. XC4003H–with 50% of the outputs simultaneously sinking 24 mA. XC4005H–with 33% of the outputs simultaneously sinking 24 mA.
With no output current loads, no active input or long line pull-resistors, all package pins at V_{cc} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed	Grade	-6	-5	-4	
Description	Symbol	Device	Max	Max	Max	Units
Full length, both pull-ups, inputs from IOB i-pins	T _{WAF}	XC4003H XC4005H	9.0 10.0	8.0 9.0	5.0 6.0	ns ns
Full length, both pull-ups inputs from internal logic	T _{WAFL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	7.0 8.0	ns ns
Half length, one pull-up inputs from IOB i-pins	T _{WAO}	XC4003H XC4005H	9.0 10.0	8.0 9.0	6.0 7.0	ns ns
Half length, one pull-up inputs from internal logic	T _{WAOL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	8.0 9.0	ns ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPR} or T_{OPC}), as listed on page 2-93.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed	d Grade	-6	-5	-4	
Description	Symbol	Device	Max	Max	Max	Units
Global Signal Distribution From pad through primary buffer, to any clock k	T _{PG}	XC4003H XC4005H	7.8 8.0	5.8 6.0	5.1 5.5	ns ns
From pad through secondary buffer, to any clock k	T _{SG}	XC4003H XC4005H	8.8 9.0	6.8 7.0	6.3 6.7	ns ns

Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

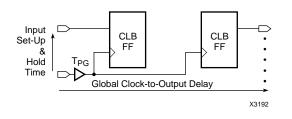
	Speed Grade			-5	
Description	Symbol	Device	Max	Max	Units
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. while T is Low, i.e. buffer is constantly active	T _{IO1}	XC4003H XC4005H	8.8 10.0	6.2 7.0	ns ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T _{IO2}	XC4003H XC4005H	9.3 10.5	6.7 7.5	ns ns
T going Low to L.L. going from resistive pull-up or float- ing High to active Low, (TBUF configured as open drain)	T _{ON}	XC4003H XC4005H	10.7 12.0	9.0 10.0	ns ns
T going High to TBUF going inactive, not driving the L.L.	T _{OFF}	All devices	3.0	2.0	ns
T going High to L.L. going from Low to High, pulled up by single resistor	T _{PUS}	XC4003H XC4005H	24.0 26.0	20.0 22.0	ns ns
T going High to L.L. going from Low to High, pulled up by two resistors	T _{PUF}	XC4003H XC4005H	11.0 12.0	9.0 10.0	ns ns

Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used, and the indirectly derived values must be ignored.

	Spee	d Grade	-6*	-5*	
Description	Symbol	Device			Units
Global Clock to Output (fast) using nearest CLB FF	Т _{IСКОF} (Max)	XC4003H XC4005H			ns ns
Global Clock to Output (slew limited) using nearest CLB FF	Т _{іСКО} (Max)	XC4003H XC4005H			ns ns
Input Set-up Time, using nearest CLB FF	T _{PSUF} (Min)	XC4003H XC4005H			ns ns
Input Hold time, using nearest CLB FF	T _{PHF} (Min)	XC4003H XC4005H			ns ns

* Data not available at press time



Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching.

These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature,

and also with the most unfavorable clock polarity choice. The use of a rising-edge clock reduces the effective clock delay by 1 to 2 ns.

The use of a rising clock edge, therefore, reduces the clock-to-output delay, and ends the hold-time requirement earlier. The use of a falling clock edge reduces the input set-up time requirement.

In the tradition of guaranteeing absolute worst-case parameter values, the table above does not take advantage of these improvements. The user can chose between a rising clock edge with slightly shorter output delay, or a falling clock edge with slightly shorter input set-up time. One of these parameters is inevitably better than the guaranteed specification listed above, albeit by only one to two nanoseconds.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade			-{	5	
Description	Symbol			Min Max		Units
Combinatorial Delays F/G inputs to X/Y outputs F/G inputs via H' to X/Y outputs C inputs via H' to X/Y outputs	T _{ILO} T _{IHO} T _{HHO}		6.0 8.0 7.0		4.5 7.0 5.0	ns ns ns
CLB Fast Carry Logic Operand inputs (F1,F2,G1,G4) to C_{OUT} Add/Subtract input (F3) to C_{OUT} Initialization inputs (F1,F3) to C_{OUT} C_{IN} through function generators to X/Y outputs C_{IN} to C_{OUT} , bypass function generators.	T _{OPCY} T _{ASCY} T _{INCY} T _{SUM} T _{BYP}		7.0 8.0 6.0 8.0 2.0		5.5 6.0 4.0 6.0 1.5	ns ns ns ns ns
Sequential Delays Clock K to outputs Q	Тско		5.0		3.0	ns
Set-up Time before Clock K F/G inputs F/G inputs via H' C inputs via H1 C inputs via DIN C inputs via EC C inputs via S/R, going Low (inactive) C _{IN} input via F'/G' C _{IN} input via F'/G' and H'	T _{ICK} T _{IHCK} T _{HHCK} T _{DICK} T _{ECCK} T _{RCK}	6.0 8.0 7.0 4.0 7.0 6.0 8.0 10.0		4.5 6.0 5.0 3.0 4.0 4.5 6.0 7.5		ns ns ns ns ns ns ns ns
Hold Time after Clock K F/G inputs F/G inputs via H' C inputs via H1 C inputs via DIN C inputs via EC C inputs via S/R, going Low (inactive)	T _{CKI} T _{CKIH} T _{CKHH} T _{CKEC} T _{CKR}	0 0 0 0 0 0		0 0 0 0 0		ns ns ns ns ns ns
Clock Clock High time Clock Low time	T _{CH} T _{CL}	5.0 5.0		4.0 4.0		ns ns
Set/Reset Direct Width (High) Delay from C inputs via S/R, going High to Q	T _{RPW} T _{RIO}	5.0	9.0	4.0	8.0	ns ns
Master Set/Reset* Width (High or Low) Delay from Global Set/Reset net to Q	T _{MRW} T _{MRQ}	21.0	33.0	18.0	31.0	ns ns

* Timing is based on the XC4005H. For other devices see XACT timing calculator.

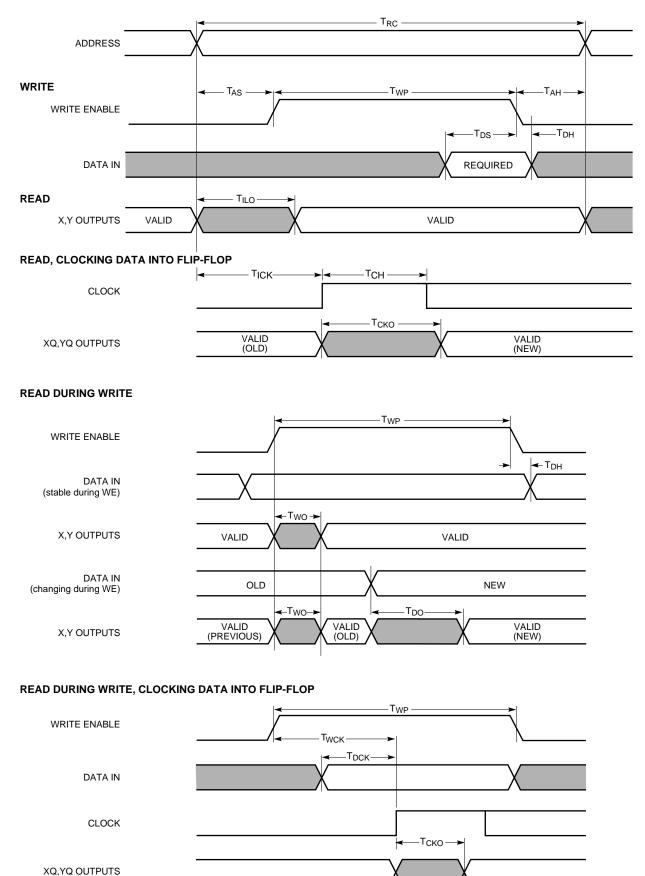
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM Option	M Option Speed Gr		-(6		5	
Description	Syn	Symbol		Max	Min	Max	Units
Write Operation							
Address write cycle time	16 x 2	T _{WC}	9.0		8.0		ns
•	32 x 1	T _{WCT}	9.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T _{WP}	5.0		4.0		ns
	32 x 1	T _{WPT}	5.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T _{AS}	2.0		2.0		ns
	32 x 1	T _{AST}	2.0		2.0		ns
Address hold time after end of WE	16 x 2	T _{AH}	2.0		2.0		ns
	32 x 1	T _{AHT}	2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T _{DS}	4.0		4.0		ns
	32 x 1	T _{DST}	5.0		5.0		ns
DIN hold time after end of WE	both	T _{DHT}	2.0		2.0		ns
Read Operation							
Address read cycle time	16 x 2	T _{RC}	7.0		5.5		ns
	32 x 1	T _{RCT}	10.0		7.5		ns
Data valid after address change	16 x 2	T _{ILO}		6.0		4.5	ns
(no Write Enable)	32 x 1	T _{IHO}		8.0		7.0	ns
Read Operation, Clocking Data into Flip-Flop							
Address setup time before clock K	16 x 2	T _{ICK}	6.0		4.5		ns
	32 x 1	TIHCK	8.0		6.0		ns
Read During Write							
Data valid after WE going active	16 x 2	T _{WO}		12.0		10.0	ns
(DIN stable before WE)	32 x 1	T _{WOT}		15.0		12.0	ns
Data valid after DIN	16 x 2	T _{DO}		11.0		9.0	ns
(DIN change during WE)	32 x 1	T _{DOT}		14.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop							
WE setup time before clock K	16 x 2	Т _{WCK}	12.0		10.0		ns
	32 x 1	T _{WCKT}	15.0		12.0		ns
Data setup time before clock K	16 x 2	T _{DCK}	11.0		9.0		ns
	32 x 1	T _{DCKT}	14.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



X2640

IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Inputs

	-6 -5					
Description	Symbol	Min	Мах	Min	Max	Units
Propagation Delays from CMOS or TTL Levels Pad to I1, I2	T _{PID}		4.0		3.0	ns

Outputs

		-6		-5		
Description	Symbol	Min	Max	Min	Мах	Units
Propagation Delays to TTL Levels						
Output (O) to Pad (Resistive Mode)	T _{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T _{OPC}		10.5		8.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T _{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T _{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T _{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T _{TSONC}		16.0		12.0	ns
Propagation Delays to CMOS Levels						
Output (O) to Pad (Resistive Mode)	T _{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T _{OPC}		9.0		7.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T _{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T _{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T _{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T _{TSONC}		14.0		11.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

2. Output delays change with capacitive loading as described in the following table.

	TTL Levels	CMOS Levels	Units
Resistive Mode	0.03	0.03	ns/pF
Capacitive Mode	0.04	0.03	ns/pF

3. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor, or alternatively, configured as a driven output or be driven from an external source.

XC4003H Pinouts

UPOMM<	Pin Description	PG191	PQ208	Bound Scan	Pin Description	PG191	PQ208	Bound Scan	Pin Description	PG191	PQ208	Bound Scan	Pin Description	PG191	PQ208	Bound Scan
IDC AGNJZ102103100K182100K182100K183100K143100 <t< td=""><td>VCC</td><td>J4</td><td>183</td><td>-</td><td>I/O</td><td>C10</td><td>27</td><td>182</td><td>GND</td><td>K15</td><td>79</td><td>-</td><td>GND</td><td>R9</td><td>131</td><td>_</td></t<>	VCC	J4	183	-	I/O	C10	27	182	GND	K15	79	-	GND	R9	131	_
INOJIJIJIJIOJIIJIOJIIJIOJIIJIOJIIJIOJIIJIIJIOJIIJIIJIIIJIIIJIIIIJIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	I/O (A8)	J3	184	62	I/O	B10	28	185	I/O	K16	80	307	I/O (D3)	T9	132	427
IDOHI18774IDOAII31194IDOLIB83316IDOV3135432UOH318874IDOAII23197IDOLIDLIDLIDLIDLIDLIDUON3422UOAII30R0AII33200IDOM1886325IDON3420UOFI19380R0OAII33202IDOM1886331IDOV5133442UOFI19380CROCID18380210CIDM1888331IDOV5143447UOFI19364CIDAII333222IDOM1690-IDO16144446UOCI19394CIDCII414222IDOM1690-IDO16144446UOCI19394IDOCII414222IDOM1690-IDO10016144446UDCI19344100AII4222IDOM169023IDO10010144450UD10011643422IDOM16100M168334IDO10010144450UD100	I/O (A9)	J2	185	65	I/O	A9	29	188	I/O	K17	81	310	I/O (RS)	U9	133	430
INOH2H2H2H2H0C11H2H37H0L0L17E4H30L00L16E5H21H30 <th< td=""><td>I/O</td><td>J1</td><td>186</td><td>68</td><td>I/O</td><td>A10</td><td>30</td><td>191</td><td>I/O</td><td>K18</td><td>82</td><td>313</td><td>I/O</td><td>V9</td><td>134</td><td>433</td></th<>	I/O	J1	186	68	I/O	A10	30	191	I/O	K18	82	313	I/O	V9	134	433
IUOH3H30T7UOB1A3A20UOL16B5C22UOT5H32A42IUOF1H32B6UOA12S4203UOM18B6328UOUOU7180448UOF1H32B6UOA1336208UOM18B6328UOUOU7180448UOF1H32B6UOA1336208UOM16B0348UOUOU6446444GNDD1H3H3C1227CNDM16B034GNDUOU644444GNDD1H3H3H3H3H3H3H4H444	I/O	H1	187	71	I/O	A11	31	194	I/O	L18	83	316	I/O	V8	135	436
ID ID AD ID AD AD AD AD <td>I/O</td> <td>H2</td> <td>188</td> <td>74</td> <td>I/O</td> <td>C11</td> <td>32</td> <td>197</td> <td>I/O</td> <td>L17</td> <td>84</td> <td>319</td> <td>I/O</td> <td>U8</td> <td>136</td> <td>439</td>	I/O	H2	188	74	I/O	C11	32	197	I/O	L17	84	319	I/O	U8	136	439
IDD (A11) G2 G3 G3 <thg3< th=""> G3 G3 <t< td=""><td>I/O</td><td>H3</td><td>189</td><td>77</td><td>I/O</td><td>B11</td><td>33</td><td>200</td><td>I/O</td><td>L16</td><td>85</td><td>322</td><td>I/O</td><td>T8</td><td>137</td><td>442</td></t<></thg3<>	I/O	H3	189	77	I/O	B11	33	200	I/O	L16	85	322	I/O	T8	137	442
IVO FI 192 68 IVO A13 66 293 IGND EI 37 6ND CIC 37 2 100 18 89 331 100 16 143 45 IGND F2 195 52 100 A14 39 216 100 NT 81 323 100 VC 143 457 100 CI 197 58 100 A14 43 227 100 78 33 100 VC 143 457 100 CI 197 58 100 116 100 <	I/O (A10)	G1	190	80	I/O	A12	34	203	I/O	M18	86	325	I/O (D2)	V7	138	445
I/OE11938960/OC1237I/OPI889334I/OU/O1/44445GNDD119695100A1439215100N/1690371007141337I/OD119695100A1439215100R1892340100V/314244440I/OD2198100C131714221100R1893343100V/314244440I/OD2200010C134742224100R1893343100V/314244480I/OD220100C134742224100R17863241001646466I/OD3100A1746232100R178633410010116478I/O10310411011011443430100116481430478I/O12022011011011443423010011681883340100116416I/O110 <td>I/O (A11)</td> <td>G2</td> <td>191</td> <td>83</td> <td>I/O</td> <td>B12</td> <td>35</td> <td>206</td> <td>I/O</td> <td>M17</td> <td>87</td> <td>328</td> <td>I/O</td> <td>U7</td> <td>139</td> <td>448</td>	I/O (A11)	G2	191	83	I/O	B12	35	206	I/O	M17	87	328	I/O	U7	139	448
GND G3 194 - I/O B13 38 212 GND M16 60. - GND T7 142 - I/O F2 195 92 I/O A14 39 216 I/O N/O 18 92 337 I/O V/O V/O V/O V/O 18 92 340 I/O V/O V/O 18 93 340 I/O V/O 16 42 224 I/O V/O 17 94 346 I/O 1/O	I/O	F1	192	86	I/O	A13	36	209	I/O	N18	88	331	I/O	V6	140	451
I/O F2 f95 92 I/O AtA 39 215 I/O N17 91 337 I/O V5 4.3 457 I/O C1 197 98 307 I/O 18 93 345 I/O V/O 14 420 1/O R18 92 340 I/O V/O 14 420 I/O F3 190 100 814 42 224 I/O N16 93 343 I/O V/O 14 480 I/O B1 420 224 110 I/O C14 45 233 I/O N16 93 365 I/O V/O V/O 14 47 480 I/O B1 47 480 230 I/O N16 101 160 N17 48 420 I/O 160 160 160 160 160 160 160 160 160 <t< td=""><td>I/O</td><td>E1</td><td>193</td><td>89</td><td>GND</td><td>C12</td><td>37</td><td>_</td><td>I/O</td><td>P18</td><td>89</td><td>334</td><td>I/O</td><td>U6</td><td>141</td><td>454</td></t<>	I/O	E1	193	89	GND	C12	37	_	I/O	P18	89	334	I/O	U6	141	454
I/O D1 196 96 I/O C1 197 86 I/O C1 197 86 I/O C1 197 86 I/O E2 198 100 C13 41 221 I/O R13 199 104 I/O R13 199 104 I/O R13 100 A16 43 227 I/O R13 100 A16 43 223 I/O N16 85 349 I/O 143 449 I/O R13 100 A17 46 230 I/O N16 95 349 I/O 143 450 I/O R13 100 A17 46 230 I/O N16 95 340 I/O 140 470 470 I/O R20 200 I/O R16 200 R16 100 361 100 140<	GND	G3	194	_	I/O	B13	38	212	GND	M16	90	_	GND	T7	142	_
IO C1 197 98 IIO C13 41 221 I/O T18 93 343 I/O U.O U.O 45 463 I/O F3 199 101 I/O A16 220 I/O No A16 220 I/O No A16 220 I/O No A16 44 220 I/O No A17 45 230 I/O RD RD NO RD NO RD NO A17 45 230 I/O RD NO RD ND RD ND RD ND RD ND RD ND RD ND ND RD ND ND RD ND ND ND ND ND ND ND ND	I/O	F2	195	92	I/O	A14	39	215	I/O	N17	91	337	I/O	V5	143	457
IVO E2 198 101 IVO B14 42 224 IVO A12 F3 199 104 IVO A16 43 227 IVO B1 200 107 IVO B15 44 230 IVO T17 96 352 IVO VA 148 472 IVO E3 202 113 IVO A17 46 230 IVO T17 96 352 IVO VA 472 VA 472 IVO E2 201 116 IVO A17 46 230 IVO VIO VIO VA 472 VIO VIO VA 472 VIO VIO VA 472 VIO VA 472 VIO VA 472 VIO VA 472 VIO	I/O	D1	196	95	I/O	A15	40	218	I/O	R18	92	340	I/O	V4	144	460
IVO E2 198 101 IVO B14 42 224 IVO A12 F3 199 104 IVO A16 43 227 IVO B1 200 107 IVO B15 44 230 IVO T17 96 352 IVO VA 148 472 IVO E3 202 113 IVO A17 46 230 IVO T17 96 352 IVO VA 472 VA 472 IVO E2 201 116 IVO A17 46 230 IVO VIO VIO VA 472 VIO VIO VA 472 VIO VIO VA 472 VIO VA 472 VIO VA 472 VIO VA 472 VIO	I/O	C1	197	98	1/0	C13	41	221	I/O	T18	93	343	1/0	U5	145	463
IVO (A12) F3 199 104 IVO A16 43 227 IVO (A13) D2 200 107 IVO B15 44 230 IVO B1 201 110 IVO C14 45 230 IVO B1 201 110 IVO C14 45 230 IVO B1 201 110 C17 46 230 IVO R17 96 355 IVO UO T5 478 VCC D3 205 C GMD D15 49 200 100 816 101 100 366 101 100 000 103 41 41 41 41 41 410 415 41 41 CCL C C C C C C C C C C C C C C C C C C <td>I/O</td> <td>E2</td> <td>198</td> <td>101</td> <td>1/0</td> <td>B14</td> <td>42</td> <td>224</td> <td>I/O</td> <td>P17</td> <td>94</td> <td>346</td> <td>1/0</td> <td>Т6</td> <td>146</td> <td>466</td>	I/O	E2	198	101	1/0	B14	42	224	I/O	P17	94	346	1/0	Т6	146	466
IOC (A13) D2 200 170 B15 4 205 IOC A13) D2 200 170 IOC B15 44 205 IOC A13) C2 203 113 IOC A17 46 236 IOC PI6 98 356 IOC 100 116 SCCX(IOC B16 47 235 IOC PI6 98 356 IOC 116 90 361 IOC 100 116 99 361 IOC 100 101 - 100 100 101 - 100 101 - 100 101 - 100 101 - 100 101 - 100 101 - 100		F3				A16	43				95					
IVO E3 202 113 IVO A17 46 236 IVO (14) C2 203 116 SGCK2 (VO) B16 47 239 SGCK1 (A15, I/O) 52 205 17 O(M1) C15 48 243 VCC D3 205 I(M0) A18 50 2451 - 206* I(M0) A18 50 2451 100* 16 10 207* 51* DONE U17 103 105* - 106* - 106* - 107* - 155* - 106* - 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 <													I/O (RCLK-BUSY/			
IDC (A14) C2 203 116 SGCK2 (I/O) B16 47 239 SGCK1 (A15, IO) B2 204 119 O (M1) C15 48 242 SGCK1 (A15, IO) B2 204 119 O(M1) C15 48 242 GND 116 100 366 11 166 11 6 116 100 366 11 152 481 - 200* - II(M0) A18 50 245 - - - 100* - - 100* - - 105* -	I/O	B1	201	110	I/O	C14	45	233	I/O	R17	97	355	I/O	U4	149	475
SBCK1 (A115, I/O) B2 204 113 O (M1) C15 48 242 SBCK3 (I/O) T16 100 364 VCC D3 205 I/O A18 50 2451 GND D15 49 10 101 I/O 103 10 103 10 100 103 105 105 105 105 105 105 155 105 165 165 165 165 165 165 165 165 165 165 165	I/O	E3	202	113	I/O	A17	46	236	I/O	P16	98	358	I/O	T5	150	478
VCC D3 205 - - 206* - - 206* - - 206* - - 207* - - 207* - - 207* - - 207* - - 207* - - 207* - - 207* - - 207* - - 1* - - - 54* - - - - 54* - - - - 54* - - - - 55* - - - 00 00 16 100 100 16 100 16 100 16 100 16 100 16 100 16 10 11 13 100 17 160 262 100 116 1	I/O (A14)	C2	203	116	SGCK2 (I/O)	B16	47	239	I/O	U18	99	361	I/O (D0, DIN)	U3	151	481
- - 206* - I (M0) A18 50 2451 - - 207* - - 51* - DONE U17 103 - 155* - - 208* - - 52* - - 104* - - 155* - GND D4 2 - - 53* - - - 105* - - - 155* - - - 105* - - - 105* - - - 105* - - - 105* - - - 105* - - - 0 0 0 0 100	SGCK1 (A15, I/O)	B2	204	119	O (M1)	C15	48	242	SGCK3 (I/O)	T16	100	364	SGCK4 (DOUT, I/O)	T4	152	484
- - 206* - I I M00 A18 50 24f1 - - 207* - - 51* - DONE U17 103 - - 16* - - 16* - - 16* - - 16* - - 16* - - 16* - - 16* - - 16* - - 16* - - - 16* - - - 16* - - - 16* - - - 16* - - - - - - - - - - - - - - - - - 00 <	VCC	D3	205	_	GND	D15	49	-	GND	R16	101	_	CCLK	V1	153	_
- - 208* - - 52* - - 104* - - 15* - GND D4 2 - - 53* - - 105* - - 15* - GND D4 2 - - 53* - - 105* - - 15* - - - 5 - - 55* - - - 107 13 11 102 15* 10 0	_	_	206*	_	I (M0)	A18	50	245†	_	_	102*	_	VCC	R4	154	_
- 1 - 53* - GND 14 2 - 53* - GND 14 2 - - 53* - - 3* - 54* - VCC R15 106 - - 15* - PGCK1 (A6, I/O) C3 4 122 - Image: Common com	_	_	207*	-	-	_	51*	_	DONE	U17	103	_	-	_	155*	_
GND D4 2 - - 54* - - - 3* - VCC D16 55 - - 107* - D(0) U2 159 - PGCK1 (A16, I/O) C3 4 122 I/O C6 56 2461 - - 107* - O(TDO) U2 159 - I/O C3 4 122 PGCK2 (I/O) B1 57 247 PGCK3 (I/O) 116 100 370 PGCK3 (I/O) 116 100 370 PGCK3 (I/O) 116 100 370 PGCK3 (I/O) 116 110 370 I/O (A0,WS) 13 161 2 I/O C6 7 131 I/O D17 60 266 I/O 111 133 11 130 I/O 161 10 100 I/O 116 162 I/O I/O I/O 111 163 26 I/	_	_	208*	_	-	_	52*	_	-	_	104*	_	-	_	156*	_
- 3* - VCC D16 55 - - 107* - 00(TDO) U2 159 - PGCK1 (A16, I/O) C3 4 122 1(M2) C16 56 2461 PROG V18 108 - GND R3 160 - I/O K3 6 128 10(HDC) E16 58 250 PGCA3 (I/O) U16 100 370 PGCA4 (I/O, A11) 11 370 I/O (A0, WS) T3 161 2 I/O C5 7 131 I/O D17 59 253 I/O T14 111 370 I/O (A0, WS) T3 161 2 I/O C6 10 140 I/O D18 61 259 I/O V14 113 379 I/O (A3) N3 166 17 I/O K3 141 I/O L16 K3 266 I/O V14 116	_	_	1*	_	-	_	53*	-	_	_	105*	_	_	_	157*	_
PGCK1 (A16, I/O) C3 4 122 I (M2) C16 56 2461 PROC V18 108 IGND R3 160 I/O B3 6 128 IVO (HDC) E16 58 250 I/O (D7) T15 109 367 I/O (A,WS) T3 161 2 I/O C57 7 131 I/O C17 59 253 I/O T14 111 373 I/O PGCK3 (I/O) 116 110 370 I/O PGCK4 (I/O, A1) U1 162 5 I/O C66 10 140 I/O B18 61 259 I/O 113 113 373 I/O B1 61 262 I/O V16 114 323 I/O A3 166 17 I/O A3 11 143 I/O F16 63 265 I/O V113 115 385 I/O VIO <td>GND</td> <td>D4</td> <td>2</td> <td>-</td> <td>_</td> <td>_</td> <td>54*</td> <td>_</td> <td>VCC</td> <td>R15</td> <td>106</td> <td>_</td> <td>-</td> <td>_</td> <td>158*</td> <td>_</td>	GND	D4	2	-	_	_	54*	_	VCC	R15	106	_	-	_	158*	_
PGCK1 (A16, I/O) C3 4 122 I(M2) C16 56 24ft PROG V18 108 GND R3 160 I/O B3 6 128 PGCK2 (I/O) B17 57 247 V/O (D7) T15 109 367 V/O (A) V/O A 16 2 I/O C53 7 131 V/O (D7) 116 100 370 PGCK4 (I/O, A1) U1 162 5 I/O A4 131 V/O C17 59 253 V/O U15 112 376 V/O PGCK4 (UO, A1) U1 162 5 I/O A4 140 V/O B18 61 259 V/O V/O 113 379 V/O (A3) N3 166 17 I/O A5 12 146 V/O F16 63 265 V/O 113 115 385 V/O 13 100 </td <td>_</td> <td>_</td> <td>3*</td> <td>_</td> <td>VCC</td> <td>D16</td> <td>55</td> <td>-</td> <td>_</td> <td>_</td> <td>107*</td> <td>_</td> <td>O (TDO)</td> <td>U2</td> <td>159</td> <td>_</td>	_	_	3*	_	VCC	D16	55	-	_	_	107*	_	O (TDO)	U2	159	_
I/O B3 6 128 I/O (HDC) E16 58 250 PGCK3 (I/O) U16 110 370 PGCK4 (I/O, A1) U1 162 5 I/O C5 7 131 I/O C17 59 253 I/O T14 111 373 I/O PGCK4 (I/O, A1) U1 162 5 I/O C5 7 131 I/O D17 60 256 I/O T14 111 373 I/O R2 164 11 I/O C6 10 140 I/O B18 61 259 I/O V16 114 379 I/O N3 166 17 I/O A3 149 I/O C18 64 268 I/O V16 114 384 I/O N2 176 20 116 100 N2 170 29 I/O A4 15 152 GND G16 67	PGCK1 (A16, I/O)	C3	4	122	I (M2)	C16	56	246†	PROG	V18	108	_	GND	R3	160	_
I/O B3 6 128 I/O (HDC) E16 58 250 PGCK3 (I/O) U16 110 370 PGCK4 (I/O, A1) U1 162 5 I/O C5 7 131 I/O C17 59 253 I/O T14 111 373 I/O PGCK4 (I/O, A1) U1 162 5 I/O C5 7 131 I/O D17 60 256 I/O T14 111 373 I/O R2 164 11 I/O C6 10 140 I/O B18 61 259 I/O V16 114 379 I/O N3 166 17 I/O A3 149 I/O C18 64 268 I/O V16 114 384 I/O N2 176 20 116 100 N2 170 29 I/O A4 15 152 GND G16 67	I/O (A17)	C4	5	125	PGCK2 (I/O)	B17	57			T15	109	367	I/O (A0, WS)	Т3	161	2
I/O C5 7 131 I/O C17 59 253 I/O T14 111 373 I/O P3 163 8 I/O (TDI) A2 8 134 I/O D17 60 256 I/O U15 112 376 I/O R2 164 11 I/O C6 10 140 I/O B18 61 256 I/O VI 113 379 I/O R2 164 11 I/O C6 10 140 I/O B18 61 256 I/O VI 113 379 I/O<(C31, A2)	I/O	B3	6	128	I/O (HDC)	E16	58	250	PGCK3 (I/O)	U16	110	370	PGCK4 (I/O, A1)	U1	162	5
I/O (TDI) A2 8 134 I/O (TCK) B4 9 137 I/O (CCK) A3 11 140 I/O A3 11 143 I/O B5 12 146 I/O B6 13 149 I/O B6 13 149 I/O A4 15 152 GND C7 14 - I/O A5 16 155 I/O A66 18 616 67 - I/O A66 18 161 60 261 I/O A66 18 161 170 20 I/O A68 19 164 170 283 I/O A68 19 164 170 289 I/O A68 19 164 170 284 170 170 283 I/O A70 88 21 170 170 284 170	I/O	C5	7	131	I/O	C17	59	253	. ,	T14	111	373	1/0	P3	163	8
I/O (TCK) B4 9 137 I/O B18 61 259 I/O C6 10 140 I/O LO E17 62 262 I/O V16 114 329 I/O (CS1, A2) T2 165 14 I/O A3 11 143 I/O F16 63 265 I/O T13 115 385 I/O A2 167 20 I/O B6 13 149 I/O C18 64 268 I/O V13 115 385 I/O R1 168 23 I/O B6 13 149 I/O C18 64 268 I/O V14 118 384 I/O R1 169 26 GND C7 14 - I/O F17 66 274 I/O V14 118 394 I/O R1 169 26 I/O A5 16 155 I/O E18 68 277 I/O V13 121 100 1	I/O (TDI)	A2	8	134	1/0		60		I/O	U15			1/0			11
I/O C6 10 140 I/O A3 11 143 I/O A3 11 143 I/O B5 12 146 I/O B6 13 149 I/O A4 15 152 GND C7 14 - I/O A4 15 152 I/O KIO F17 66 274 I/O KIO F18 69 280 I/O KIO F18 69 280 I/O KIO F18 69 280 I/O KIO F18 70 283 I/O KIO F18 70 283 I/O K	. ,															14
I/O A3 11 143 I/O B5 12 146 I/O B6 13 149 I/O B6 13 149 I/O A4 15 152 GND C7 14 - I/O A4 15 152 I/O K1 66 274 I/O A4 15 152 I/O K1 66 7 - I/O K1 166 67 - I/O K1 166 67 - I/O V13 120 397 I/O K1 166 67 - I/O V13 120 397 I/O K18 68 277 I/O V10 V13 120 397 I/O K18 616 67 - I/O V13 121 400 I/O K18 616 77 283 I/O V13 121 400 I/O K18 <td>. ,</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>. ,</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	. ,								. ,							
I/O B5 12 146 I/O C18 64 268 I/O B6 13 149 I/O D18 65 271 II 116 388 I/O R1 169 26 GND C7 14 - I/O F17 66 274 I/O V14 118 394 I/O R1 169 26 I/O A4 15 152 GND G16 67 - I/O V14 118 394 I/O R1 169 26 I/O A5 16 155 I/O E18 68 277 I/O V13 120 397 I/O R1 170 23 I/O A6 18 161 I/O G17 70 283 I/O V13 121 400 I/O N1 175 41 I/O A6 18 161 I/O G18 71 286 I/O V12 123 406 I/O I/O A1					. ,								. ,			
I/O B6 13 149 I/O D18 65 271 GND C7 14 - I/O F17 66 274 I/O A4 15 152 GND G16 67 - I/O A5 16 155 I/O E18 68 277 I/O A5 16 155 I/O E18 68 277 I/O A6 18 161 I/O F18 69 280 I/O C8 19 164 I/O G18 71 283 I/O C8 161 I/O G18 71 286 I/O K8 21 170 K16 72 289 I/O K8 21 170 K16 73 </td <td></td> <td>B5</td> <td></td> <td>T1</td> <td></td> <td></td>		B5												T1		
GND C7 14 - I/O A4 15 152 I/O A5 16 155 I/O A5 16 155 I/O A5 16 155 I/O A6 18 161 I/O A6 18 161 I/O 618 71 283 I/O A7 20 167 1/O 218 289 I/O 112 120 397 I/O A8 22 167 I/O 618 71 283 I/O 121 400 I/O 10 173 35 I/O A8 22 173 I/O H16 72 289 I/O 11 125 412 I/O I/O 14 178 50 I/O A8 22 173																
I/O A4 15 152 GND G16 67 - I/O A5 16 155 I/O E18 68 277 I/O U3 120 397 I/O P1 172 32 I/O A6 18 161 I/O F18 69 280 I/O V13 121 400 I/O P1 172 32 I/O A6 18 161 I/O G17 70 283 I/O V13 121 400 I/O N1 173 35 I/O A6 18 161 I/O G18 71 283 I/O V12 123 400 I/O M1 175 41 I/O A7 20 167 I/IO R18 72 289 I/O V11 124 409 I/O I/O 13 176 41 I/O A8 22 173 I/O J18 75 298 I/O V11 126 415 I/O																
I/O A5 16 155 I/O E18 68 277 I/O (TMS) B7 17 158 I/O F18 69 280 I/O V13 121 400 I/O N1 173 35 I/O A6 18 161 I/O G17 70 283 I/O V13 121 400 I/O N1 173 35 I/O C8 19 164 I/O G18 71 286 I/O V12 123 406 I/O M1 175 41 I/O A7 20 167 I/O G18 71 286 I/O V11 124 409 I/O<(A4)												_				_
I/O (TMS) B7 17 158 I/O F18 69 280 I/O V13 121 400 I/O N1 173 35 I/O A6 18 161 I/O G17 70 283 I/O V13 121 400 I/O N1 173 35 I/O C8 19 164 I/O G18 71 286 I/O V12 123 406 I/O (A4) M2 174 38 I/O A7 20 167 I/O G18 71 289 I/O (CS0) V12 123 406 I/O (A4) M2 174 38 I/O A7 20 167 I/O H16 72 289 I/O T11 124 409 I/O (A5) M1 175 41 I/O A8 22 173 I/O H18 74 295 I/O V11 126 415 I/O I/O I/I 178 50 I/O E8 2.4 179<												397				32
NO A6 18 161 I/O G17 70 283 I/O C8 19 164 I/O G18 71 283 I/O (D5) U12 122 403 I/O (A4) M2 174 38 I/O A7 20 167 I/O G18 71 286 I/O (D5) U12 122 403 I/O (A4) M2 174 38 I/O A7 20 167 I/O G18 71 286 I/O (CS0) V12 123 406 I/O (A5) M1 175 41 I/O B8 21 170 III 73 292 I/O U11 125 412 I/O L3 176 44 I/O A8 22 173 I/O H18 74 295 I/O V11 126 415 I/O L1 178 50 I/O GND D9 25 - I/O J17 76 301 I/O I10 128 421 I/O<																
I/O C8 19 164 I/O G18 71 286 I/O (CS0) V12 123 406 I/O (A5) M1 175 41 I/O A7 20 167 I/O H16 72 289 I/O T11 124 409 I/O L3 176 44 I/O A8 22 173 I/O H18 74 295 I/O V11 125 412 I/O L2 177 47 I/O A8 22 173 I/O H18 74 295 I/O V11 126 415 I/O L1 178 50 I/O C9 24 179 I/O J17 76 301 I/O V10 128 421 I/O C9 24 179 I/O J17 76 301 I/O V10 128 421 I/O C18R, INIT J16 77 304 I/O T10 129 424 I/O K3 181 59																
I/O A7 20 167 I/O H16 72 289 I/O T11 124 409 I/O L3 176 44 I/O B8 21 170 I/O H17 73 292 I/O U/O																
I/O B8 21 170 H17 73 292 I/O U1 125 412 I/O L2 177 47 I/O A8 22 173 I/O H18 74 295 I/O V11 126 412 I/O L1 178 50 I/O B9 23 176 I/O J18 75 298 I/O V10 127 418 I/O L1 178 50 I/O C9 24 179 I/O J17 76 301 I/O V10 128 421 I/O K1 179 53 GND D9 25 - I/O<(ERR, ĪNĪT)									. ,							
I/O A8 22 173 I/O H18 74 295 I/O V11 126 415 I/O L1 178 50 I/O B9 23 176 I/O J18 75 298 I/O V10 127 418 I/O K1 179 53 I/O C9 24 179 I/O J17 76 301 I/O V10 128 421 I/O K1 179 53 GND D9 25 - I/O(ERR, ĪNĪT) J16 77 304 I/O T10 129 424 I/O(A7) K3 181 59																
I/O B9 23 176 I/O J18 75 298 I/O V10 127 418 I/O K1 179 53 I/O C9 24 179 I/O J17 76 301 I/O (D4) U10 128 421 I/O (A6) K2 180 56 GND D9 25 - I/O (ERR, ĪNĪT) J16 77 304 I/O T10 129 424 I/O (A7) K3 181 59																
I/O C9 24 179 I/O J17 76 301 I/O (D4) U10 128 421 I/O (A6) K2 180 56 GND D9 25 - I/O (ERR, INIT) J16 77 304 I/O (D4) U10 128 421 I/O (A6) K2 180 56																
GND D9 25 - I/O (ERR, ĪNĪT) J16 77 304 I/O T10 129 424 I/O (A7) K3 181 59																
	VCC	D9 D10	25 26	-		J16	78	- 304	vcc	R10	129	424	GND	K3 K4	181	- 59

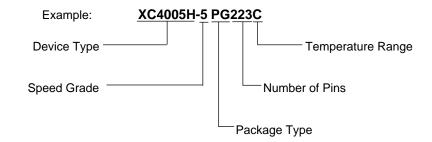
* Indicates unconnected package pins. † Contributes only one bit (.i) to the boundary scan register. Boundary Scan Bit 0 = TDO.T Boundary Scan Bit 1 = TDO.O Boundary Scan Bit 487 = BSCANT.UPD

XC4005H Pinouts

Pin	Dom	MODAG	Bound	Pin	Bom	MODAD	Bound Scan	Pin	Dom	MODAD	Bound	Pin Description	Bom	MODA	Bound
Description VCC	PG223 J4	MQ240 212	Scan _	Description I/O	PG223 B10	MQ240 32	Scan 221	Description I/O	PG223 K16	MQ240 92	Scan 367	I/O (D3	PG223 T9	MQ240 152	Scan 511
I/O (A8)	J4 J3	212	- 74	1/O	A9	32	221	1/O	K16	92	307	I/O (D3	U9	152	511
I/O (A9)	J2	213	77	1/O	A10	34	227	1/O	K18	94	373	1/O	V9	154	517
1/O (A9)	J2 J1	214	80	1/O	A10	35	230	1/O	L18	94	376	1/0	V9 V8	155	520
1/O	H1	216	83	1/O	C11	36	233	1/O	L17	96	379	1/0	U8	156	523
I/O	H2	217	86	GND	-	37		I/O	L16	97	382	I/O	T8	157	526
I/O	H3	218	89	I/O	D11	38	236	GND	-	98	-	GND		158	
GND	-	219	-	I/O	D12	39	239	I/O	L15	99	385	I/O (D2)	V7	159	529
I/O (A10)	G1	220	92	VCC	-	40	-	I/O	M15	100	388	I/O	U7	160	532
I/O (A11)	G2	221	95	I/O	B11	41	242	VCC	:	101	-	VCC	-	161	-
VCC	-	222	-	I/O	A12	42	245	I/O	M18	102	391	I/O	V6	162	535
I/O	H4	223	98	I/O	B12	43	248	I/O	M17	103	394	I/O	U6	163	538
I/O	G4	224	101	I/O	A13	44	251	I/O	N18	104	397	I/O	R8	164	541
I/O	F1	225	104	GND	C12	45	-	I/O	P18	105	400	I/O	R7	165	544
I/O	E1	226	107	I/O	D13	46	254	GND	M16	106	-	GND	T7	166	-
GND	G3	227	-	I/O	D14	47	257	I/O	N15	107	403	1/0	R6	167	547
1/0	F2	228	110	I/O	B13	48	260	I/O	P15	108	406	1/0	R5	168	550
1/0	D1	229	113	I/O	A14	49	263	I/O	N17	109	409	1/0	V5	169	553
1/0	C1 E2	230	116	I/O	A15	50	266	I/O	R18	110	412	1/0	V4	170	556
I/O		231	119	I/O	C13	51	269	I/O	T18	111	415	1/0	U5	171	559
I/O (A12)	F3 D2	232	122	I/O I/O	B14	52 53	272 275	I/O I/O	P17	112	418	I/O I/O (D1)	T6 V3	172 173	562
I/O (A13)	DZ	233	125	1/0	A16	53	2/5	1/0	N16	113	421	I/O (D1)	V3	173	565
I/O	F4	234	128	I/O	B15	54	278	I/O	T17	114	424	RDY)	V2	174	568
I/O	E4	235	131	I/O	C14	55	281	I/O	R17	115	427	I/O	U4	175	571
I/O	B1	236	134	I/O	A17	56	284	I/O	P16	116	430	I/O	T5	176	574
I/O	E3	237	137	SGCK2 (I/O)	B16	57	287	I/O	U18	117	433	I/O (D0, DIN)	U3	177	577
I/O (A14)	C2	238	140	O (M1)	C15	58	290	SGCK3 (I/O)	T16	118	436	SGCK4 (DOUT, I/O)	T4	178	580
SGCK1 (A15, I/O)	B2	239	143	GND	D15	59	-	GND	R16	119	-	CCLK	V1	179	-
VCC	D3	240	-	I (M0)	A18	60	293†	DONE	U17	120	-	VCC	R4	180	-
GND	D4	1	-	VCC	D16	61	-	VCC	R15	121	-	O (TDO)	U2	181	-
PGCK1 (A16,I/O)	C3	2	146	I (M2)	C16	62	294†	PROG	V18	122	-	GND	R3	182	-
I/O (A17)	C4	3	149	PGCK2 (I/O)	B17	63	295	I/O (D7)	T15	123	439	I/O (A0, WS)	T3	183	2
I/O	B3	4	152	I/O (HDC)	E16	64	298	PGCK3 (I/O)	U16	124	442	PGCK4 (I/O, A1)	U1	184	5
I/O	C5	5	155	I/O	C17	65	301	I/O	T14	125	445	I/O	P3	185	8
I/O (TDI)	A2	6	158	I/O	D17	66	304	I/O	U15	126	448	I/O	R2	186	11
I/O (TCK)	B4	7	161	I/O	B18	67	307	I/O	R14	127	451	I/O (CS1, A2)	T2	187	14
1/0	C6	8	164	I/O (LDC)	E17	68	310	I/O	R13	128	454	I/O (A3)	N3	188	17
1/0	A3	9	167	I/O	F16	69	313	I/O (D6)	V17	129	457	1/0	P4	189	20
1/0	B5	10	170	I/O	C18	70	316	I/O	V16	130	460	1/0	N4	190	23
1/0	B6 D5	11	173	I/O	D18	71	319	I/O	T13	131	463	1/0	P2 T1	191	26
I/O I/O	D5 D6	12 13	176 179	I/O I/O	F17 E15	72 73	322 325	I/O I/O	U14 V15	132 133	466 469	1/O 1/O	R1	192 193	29 32
GND	D6 C7	13	- 179	1/O	F15	73	325	1/O	V15	133	469	1/0 1/0	N2	193	32
I/O	A4	14	- 182	GND	G16	74		GND	T12	134	-1/2			194	
1/O	A4 A5	16	185	I/O	E18	76	331	I/O	R12	135	475	GND	 M3	195	_
I/O (TMS)	B7	17	188	1/O	F18	77	334	1/O	R11	137	478	1/0	P1	197	38
I/O	A6	18	191	1/O	G17	78	337	1/O	U13	138	481	1/0	N1	198	41
VCC	-	19	-	1/O	G18	79	340	1/O	V13	139	484	1/O	M4	199	44
1/0	D7	20	194	VCC	-	80	-	VCC	-	140	-	1/0	L4	200	47
I/O	D8	21	197	I/O	H16	81	343	I/O (D5)	U12	141	487	VCC	-	201	-
GND	-	22	-	I/O	H17	82	346	I/O (CSO)	V12	142	490	I/O (A4)	M2	202	50
I/O	C8	23	200	GND	-	83	_	GND	-	143	_	I/O (A5)	M1	203	53
I/O	A7	24	203	I/O	G15	84	349	I/O	T11	144	493	GND	-	204	-
I/O	B8	25	206	I/O	H15	85	352	I/O	U11	145	496	I/O	L3	205	56
I/O	A8	26	209	I/O	H18	86	355	I/O	V11	146	499	I/O	L2	206	59
I/O	B9	27	212	I/O	J18	87	358	I/O	V10	147	502	I/O	L1	207	62
I/O	C9	28	215	I/O	J17	88	361	I/O (D4)	U10	148	505	I/O	K1	208	65
GND	D9	29	-	I/O (ERR, INIT)	J16	89	364	I/O	T10	149	508	I/O (A6)	K2	209	68
VCC	D10	30	-	VCC	J15	90	-	VCC	R10	150	_	I/O (A7)	K3	210	71
I/O	C10	31	218	GND	K15	91	-	GND	R9	151	-	GND	K4	211	-
* Indicates unconne						•			•	•		·			

* Indicates unconnected package pins. † Contributes only one bit (.i) to the boundary scan register. Boundary Scan Bit 0 = TDO.T Boundary Scan Bit 1 = TDO.O

Ordering Information



Component Availability

PINS	84	100		120 144		156 160		164 191		196	208		223	225	240		299	
				TOP					TOP		TOP							
TYPE	PLAST.	PLAST.	PLAST.	BRAZED	CERAM.	PLAST.	CERAM	PLAST.	BRAZED	CERAM.	BRAZED	PLAST.	METAL	CERAM.	PLAST.	PLAST.	METAL	METAL
	PLCC	PQFP	VQFP	CQFP	PGA	TQFP	PGA	PQFP	CQFP	PGA	CQFP	PQFP	PQFP	PGA	BGA	PQFP	PQFP	PQFP
CODE	PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299
XC4003H -6										CI		CI						
-5										С		С						
XC4005H -6														CI		CI	CI	
-5														С		С	С	
										_								

 $C = Commercial = 0^{\circ} \text{ to } +85^{\circ} \text{ C} \qquad I = Industrial = -40^{\circ} \text{ to } +100^{\circ} \text{ C} \qquad M = Mil \text{ Temp} = -55^{\circ} \text{ to } +125^{\circ} \text{ C}$

B = MIL-STD-883C Class B Parentheses indicate future product plans