XC4000H
High I/O Count
Logic Cell Array Family

Product Specifications

Features

- Third-generation Field-Programmable Gate Arrays
  - Very high number of I/O pins
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (four per edge)
  - Efficient implementation of multi-level logic
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate with (two modes including SoftEdge)
- Per-pin individually configurable input threshold and output high level, either TTL or CMOS
  - Programmable input pull-up or pull-down resistors
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and interconnect
  - Low power consumption
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on ’386/’486-type PC, NEC PC, Apollo, Sun-4, and Hewlett Packard 700 Series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Device	XC4003H	XC4005H
Approximate Gate Count	3,000	5,000
Number of IOBs	160	192
CLB Matrix	10 x 10	14 x 14
Number of CLBs	100	196
Number of Flip-Flops	200	392
Max Decode Inputs (per side)	30	42
Max RAM Bits	3,200	6,272

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

The XC4000H family is intended for I/O-intensive applications. Compared to the XC4000, the XC4000H devices have almost double the number of IOBs and I/O pins, and offer a choice of CMOS- or TTL-level outputs and input thresholds, selectable per pin. The XC4000H outputs sink 24 mA and offer improved 3-state and slew-rate control.

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000H family is supported by the same powerful and sophisticated software as the XC4000 family, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally to the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

For a detailed description of the device features, architecture, configuration methods and pin descriptions, see pages 2-9 through 2-45.

XC4000H Compared to XC4000

For readers already familiar with the XC4000 family, here is a concise list of the major new features in the XC4000H family.

- Number of IOBs is, roughly, doubled compared to the XC4000.
- Output slew-rate control is significantly improved.

  Resistive Load means a strong pull-down all the way to ground, capable of sinking 24 mA continuously. If many outputs switch simultaneously, the resulting ground bounce might be objectionable.

  Capacitive Load, or SoftEdge, means a more sophisticated pull-down that decreases in strength as it approaches ground. It can only sink 4 mA at V_{OL}, which is irrelevant when driving capacitive loads. The benefit is a substantial reduction in ground bounce when several outputs switch simultaneously.

  In the XC4000, limiting the slew rate of the output reduces ground bounce, but also introduces a significant additional delay. In the XC4000H, the additional delay in the capacitive-load mode is usually insignificant.
- All input and output flip-flops have been eliminated in the XC4000H family. Use the CLB flip-flops instead.
- Outputs can sink 24 mA, guaranteed at V_{OL} = 0.5 V, compared to the 12 mA at 0.4 V of the XC4000 family.
- Number of decoder inputs per side
- Each output may be individually configured as one of the following.
  - TTL-compatible (like the XC4000) that uses n-channel transistors for both pull-down and pull-up,
  - A totem-pole output structure with reduced V_{OH},
  - CMOS-compatible (like the XC2000 and XC3000) that means n-channel pull-down and p-channel pull-up with V_{OH} close to the V_{CC} rail.
- Each input can individually be configured for either TTL-compatible threshold (1.2 V) or for CMOS-compatible threshold (V_{CC}/2). Each input can be configured to be inverting or non-inverting.
- Any combination of programmable input and output levels on any I/O pin is possible, even the dubious combination of TTL output and CMOS input on the same I/O pin.
- Output 3-state operation is controlled by a two-input multiplexer.
- The first activation of outputs after the end of the configuration process, as they change from 3-state to their active level, is always in the SoftEdge mode. This prevents potential ground-bounce problems when all outputs turn on simultaneously. A few nanoseconds later, each output assumes the current-sink capability determined by its configuration. This soft wake-up operation is transparent to the user.

Architectural Overview

Except for the I/O structure, the XC4000H family is identical to the original XC4000 family. A matrix of Configurable Logic Blocks is interconnected through a hierarchy of flexible routing resources. The powerful system-integration features of the XC4000 family, such as on-chip RAM, dedicated fast carry, and wide decoders, are retained in the XC4000H family.

The XC4000H family almost doubles the number of input/output pins compared to the XC4000, an attractive feature for I/O-intensive applications. The output drivers were redesigned to be more powerful and more flexible.

Input/Output Blocks (IOBs)

The IOBs form the interface between the internal logic and the I/O pads of the XC4000H device. Each IOB consists of a programmable output section that can drive the pad, and a programmable input section, that can receive data from the pad. Aside from being connected to the same pad, the input and output sections have nothing else in common.

Input

In XC4000H devices, there are no input flip-flops.

The input section receives data from the pad. Each input can be configured individually with TTL or CMOS input thresholds. As a configuration option, the input can be either inverted or non-inverted, before it is made available to the internal logic.

Pad

Each I/O pad can be configured with or without a pull-up or pull-down resistor, independent of the pin usage.

Boundary Scan

The XC4000H IOBs have the same IEE 1149.1boundary-scan capabilities as the IOBs in the original XC4000.

Output

In an XC4000H IOB, there is no output flip-flop. The output section receives data and 3-state control information from the CLB interconnect structure.

Under configuration control, the data can be inverted or non-inverted. The output driver assumes one of the following states.

- Permanently disabled, making the pad an input only pad
- 3-state controlled from the internal logic

There are two potential sources of the 3-state-control information, selected by a multiplexer. The output of the multiplexer driving the 3-state control can be inverted as a configuration option. The signal can be active High 3-state, which is identical to the more popular connotation of active-Low Output Enable, or it can be active-High Output Enable, which is identical to active Low 3-state.

Each output can be individually configured as either TTL- or CMOS-compatible. A TTL-compatible output uses n-channel transistors for both pull-down and pull-up. As a result, the output High voltage, V_{OH}, is at least one threshold voltage drop below V_{CC}. Depending on the load current, this means a voltage drop of 1.0 to 2.4 V. In a system using TTL input thresholds of 1.2 V, this lower output voltage results in shorter delays when switching from High to Low, and thus a better delay balance between the two signal directions. The smaller signal amplitude also generates less noise. The reduction in High-level noise margin is irrelevant because it is still much better than the Low-level noise margin. TTL-level outputs are, therefore, the best choice for systems that use TTL-level input thresholds. (XC4000 and XC4000A devices have only TTL-level outputs and have only TTL-level input thresholds).

When the output is configured as CMOS-compatible, an additional p-channel transistor pulls the output towards the V_{CC} rail. This results in an unloaded rail-to-rail signal swing, ideal for systems that use CMOS input thresholds. (XC2000 and XC3000 devices have only CMOS-level outputs).

Each output can be configured for either of two slew-rate options, which affect only the pull-down operation. When configured for resistive load, the pull-down transistor is driven hard, resulting in a practically constant on-resistance of about 10 Ω. This results in the fastest High-to-Low transition, and the capability to sink 24 mA with a voltage of 500 mV. When many outputs switch High to Low simultaneously, especially when they are discharging a capacitive load, this configuration option might result in excessive ground bounce.

When configured for capacitive load, or SoftEdge, the High-to-Low transition starts as described above, but the drive to the pull-down transistor is reduced as soon as the output voltage reaches a value around 1 V. This results in a higher resistance in the pull-down transistor, a slowing down of the falling edge, and a significantly reduced ground bounce.

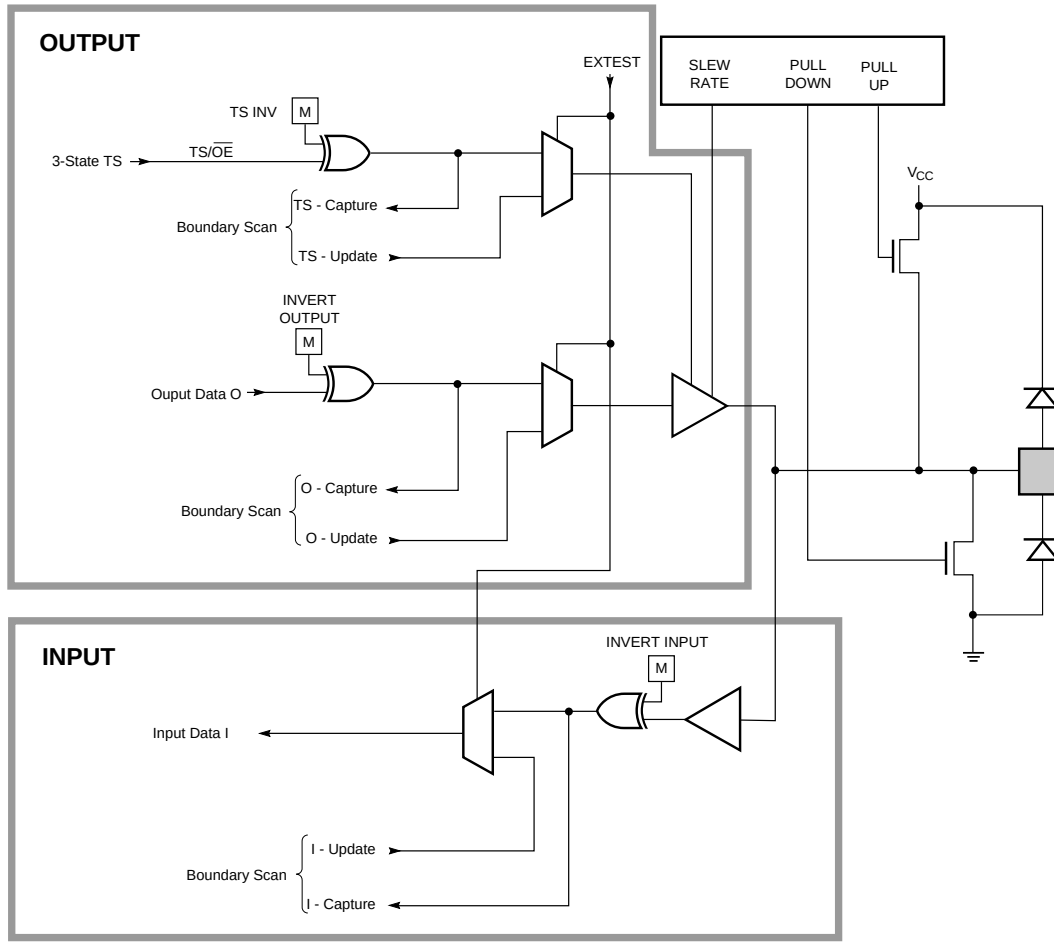


Figure 1. XC4000H Input/Output Block

Slew-Rate Control with SoftEdge

The XC4000H outputs use a novel, patent-pending method of slew-rate control that reduces ground bounce without any significant delay penalty. Each output is configured with a choice between two slew-rate options. Both options reduce the positive ground bounce that occurs when the output current is turned on. They differ in the way the output current is turned off.

- The slew-rate-limited default mode is called capacitive, or SoftEdge. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive until the output voltage has reached +1 V. The pull-down transistor is then gradually turned off, so that it finally has an on-resistance of about 100 Ω, low enough to sink 4 mA continuously. Gradually turning off the sink current reduces the max value of current change (di/dt) that is normally responsible for the negative voltage spike over the common ground inductance (bonding wires), called ground bounce.

  The capacitive, or SoftEdge, mode is the best choice for capacitively loaded outputs, or for outputs requiring less than 4 mA of dc sink current.

- The non-slew-rate limited mode is called resistive. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive as long as the output data is a logic Low. The pull-down transistor has an impedance of <20 Ω, capable of sinking 24 mA continuously.

  Resistive mode is required for driving terminated transmission lines with 4 to 24 mA of dc sink current. The abrupt current change when the output voltage reaches zero causes a voltage spike over the ground inductance (bonding wire) and can result in objectionable ground bounce when many outputs switch High-to-Low simultaneously.

The following figures show output rising and falling edges when one output drives different loads. The tests were performed on a multi-ground-plane test PC board, manufactured by Urban Instruments (Encino, CA). Measurements were done with a Tektronix TDS540 digital storage oscilloscope. The figures below are unedited files from these measurements, the time scale is 2 ns/division.

The upper trace in each figure shows a second output driven from the same internal signal, but unloaded. It acts as a timing reference, and triggers the oscilloscope.

Resistive mode and capacitive mode transitions start with practically the same delay from the internal logic. Resisitive mode falls faster, and has more undershoot; capacitive mode rises slightly faster. For a 200-Ω pull-up, 330-Ω pull-down termination, only resisitive mode is meaningful. A TTL-output with a 1000-Ω pull-up, 150-pF termination has a slow (150 ns) final rise time that extends outside the 10-ns timing window of these figures.

Trace A shows Resistive mode with CMOS outputs
Trace B shows Resistive mode with TTL outputs
Trace C shows Capacitive mode with CMOS outputs
Trace D shows Capacitive mode with TTL outputs

Summary
Use resistive mode for applications that require >4 mA of dc sink current, and for heavy capacitive loads when they must be discharged fast. Use capacitive mode for all other applications, especially for light capacitive loads (50 to 200 pF) and for all timing-uncritical outputs that require <4 mA dc current. The Low-to-High transition is not affected by the choice of slew-rate mode.

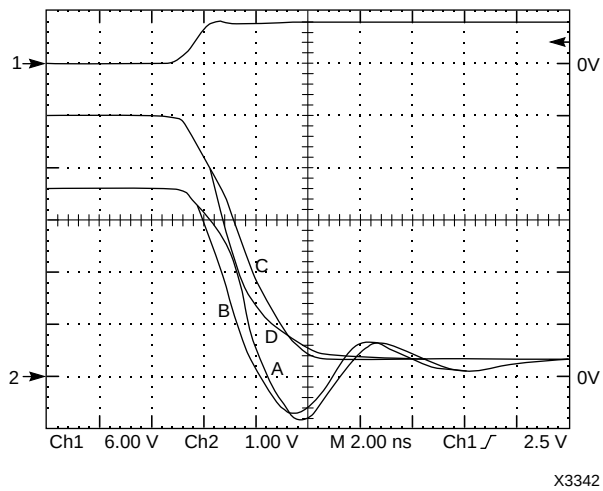


Figure 2. Falling Edge, 50 pF Load

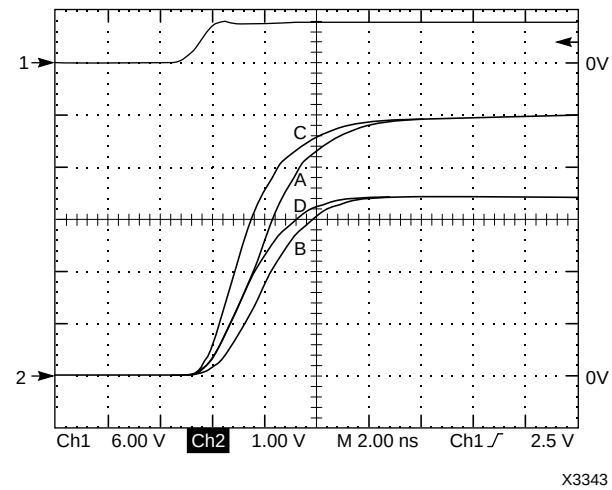


Figure 3. Rising Edge, 50 pF Load

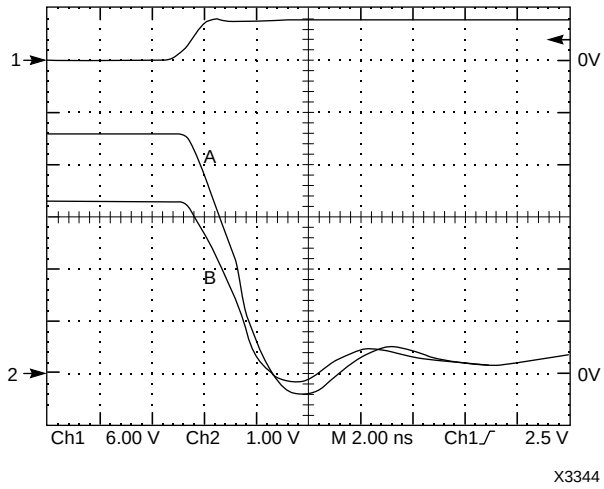


Figure 4. Falling Edge, 200/330 Ω, 50 pF Load

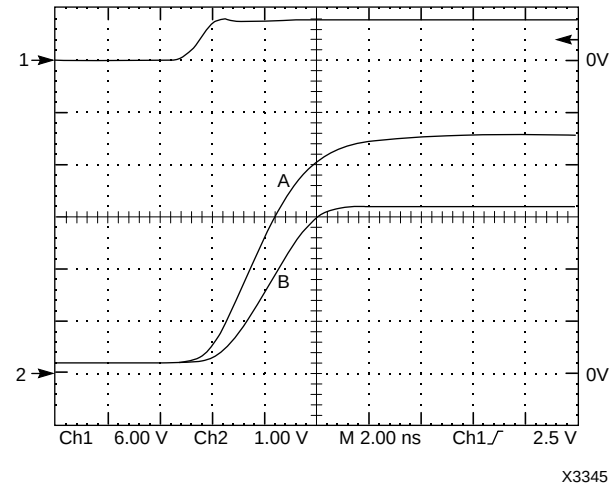


Figure 5. Rising Edge, 200/330 Ω, 50 pF Load

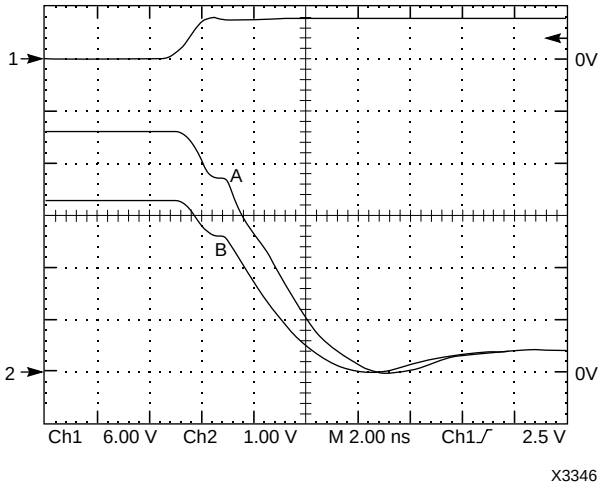


Figure 6. Falling Edge, 200/330 Ω, 150 pF Load

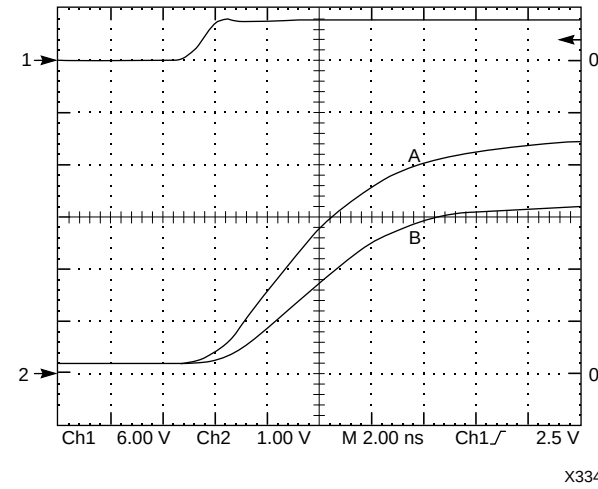


Figure 7. Rising Edge, 200/330 Ω, 150 pF Load

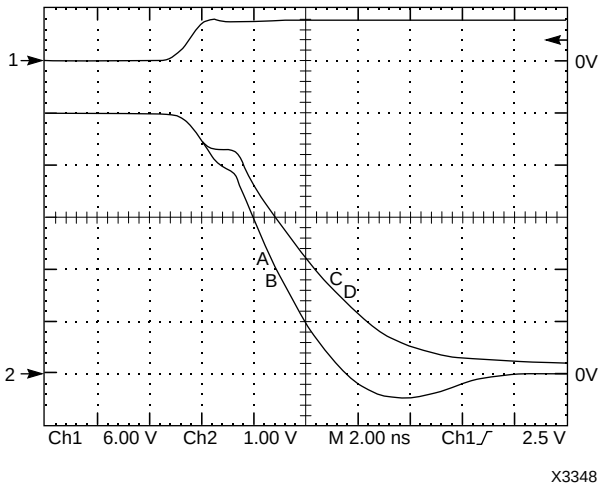


Figure 8. Falling Edge, 1000 Ω, 150 pF Load

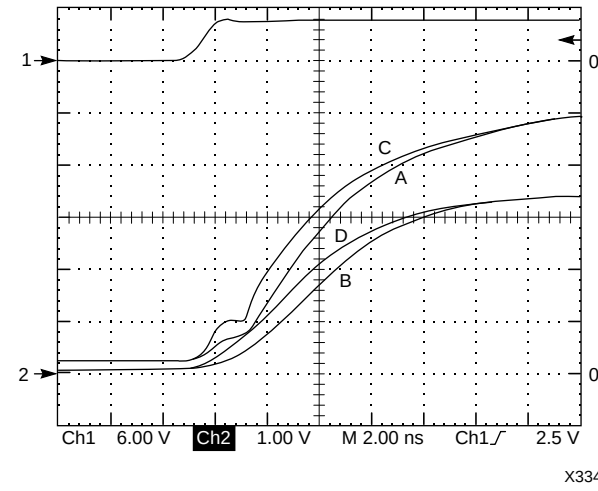


Figure 9. Rising Edge, 1000 Ω, 150 pF Load

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V_{IH}	High-level input voltage for TTL threshold	2.0	V_{CC}	V
V_{IH}	High-level input voltage for CMOS threshold	70%	100%	V_{CC}
V_{IL}	Low-level input voltage for TTL threshold	0	0.8	V
V_{IL}	Low-level input voltage CMOS threshold	0	20%	V_{CC}

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage, TTL option @ I_{OH} = –4.0 mA	2.4		V
V_{OH}	High-level output voltage, CMOS option @ I_{OH} = -1 mA	V_{CC} -0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 24 mA, V_{CC} max (Note 1)		0.5	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (estimate)	0.02	0.20	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. XC4003H–with 50% of the outputs simultaneously sinking 24 mA. XC4005H–with 33% of the outputs simultaneously sinking 24 mA.
2. With no output current loads, no active input or long line pull-resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB i-pins	T_{WAF}	XC4003H XC4005H	9.0 10.0	8.0 9.0	5.0 6.0	ns ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	7.0 8.0	ns ns
Half length, one pull-up inputs from IOB i-pins	T_{WAO}	XC4003H XC4005H	9.0 10.0	8.0 9.0	6.0 7.0	ns ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	8.0 9.0	ns ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPR} or T_{OPC}), as listed on page 2-93.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Global Signal Distribution	T_{PG}	XC4003H	7.8	5.8	5.1	ns
From pad through **primary** buffer, to any clock k		XC4005H	8.0	6.0	5.5	ns
From pad through **secondary** buffer, to any clock k	T_{SG}	XC4003H	8.8	6.8	6.3	ns
		XC4005H	9.0	7.0	6.7	ns

Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

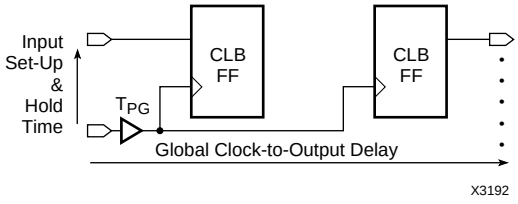
	Speed Grade		-6	-5	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4003H XC4005H	8.8 10.0	6.2 7.0	ns ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4003H XC4005H	9.3 10.5	6.7 7.5	ns ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TBUF configured as open drain)	T_{ON}	XC4003H XC4005H	10.7 12.0	9.0 10.0	ns ns
T going High to TBUF going inactive, not driving the L.L.	T_{OFF}	All devices	3.0	2.0	ns
T going High to L.L. going from Low to High, pulled up by single resistor	T_{PUS}	XC4003H XC4005H	24.0 26.0	20.0 22.0	ns ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4003H XC4005H	11.0 12.0	9.0 10.0	ns ns

Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used, and the indirectly derived values must be ignored.

	Speed Grade		-6*	-5*	
Description	**Symbol**	**Device**			**Units**
Global Clock to Output (fast) using nearest CLB FF	T_{ICKOF} (Max)	XC4003H XC4005H			ns ns
Global Clock to Output (slew limited) using nearest CLB FF	T_{ICKO} (Max)	XC4003H XC4005H			ns ns
Input Set-up Time, using nearest CLB FF	T_{PSUF} (Min)	XC4003H XC4005H			ns ns
Input Hold time, using nearest CLB FF	T_{PHF} (Min)	XC4003H XC4005H			ns ns

* Data not available at press time



Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching.

These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice. The use of a rising-edge clock reduces the effective clock delay by 1 to 2 ns.

The use of a rising clock edge, therefore, reduces the clock-to-output delay, and ends the hold-time requirement earlier. The use of a falling clock edge reduces the input set-up time requirement.

In the tradition of guaranteeing absolute worst-case parameter values, the table above does not take advantage of these improvements. The user can chose between a rising clock edge with slightly shorter output delay, or a falling clock edge with slightly shorter input set-up time. One of these parameters is inevitably better than the guaranteed specification listed above, albeit by only one to two nanoseconds.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade	-6		-5		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0	ns
CLB Fast Carry Logic						
Operand inputs (F1,F2,G1,G4) to C_{OUT}	T_{OPCY}		7.0		5.5	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		8.0		6.0	ns
Initialization inputs (F1,F3) to C_{OUT}	T_{INCY}		6.0		4.0	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5	ns
Sequential Delays						
Clock K to outputs Q	T_{CKO}		5.0		3.0	ns
Set-up Time before Clock K						
F/G inputs	T_{ICK}	6.0		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		ns
C_{IN} input via F'/G'		8.0		6.0		ns
C_{IN} input via F'/G' and H'		10.0		7.5		ns
Hold Time after Clock K						
F/G inputs	T_{CKI}	0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		ns
C inputs via H1	T_{CKHH}	0		0		ns
C inputs via DIN	T_{CKDI}	0		0		ns
C inputs via EC	T_{CKEC}	0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		ns
Clock						
Clock High time	T_{CH}	5.0		4.0		ns
Clock Low time	T_{CL}	5.0		4.0		ns
Set/Reset Direct						
Width (High)	T_{RPW}	5.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0	ns
Master Set/Reset*						
Width (High or Low)	T_{MRW}	21.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0	ns

* Timing is based on the XC4005H. For other devices see XACT timing calculator.

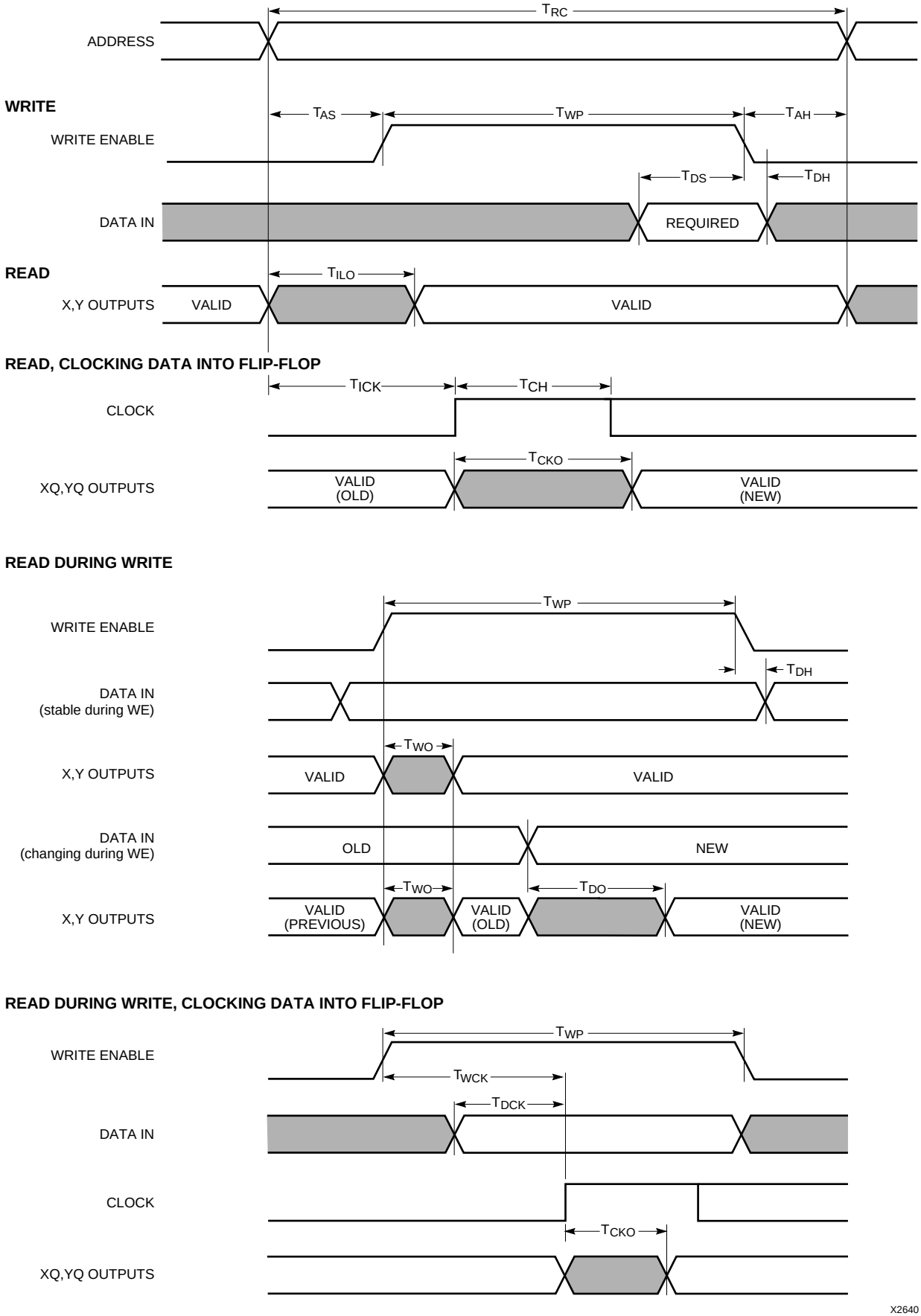
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM Option	**Speed Grade**		**-6**		**-5**		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation							
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		ns
Read Operation							
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		ns
	32 x 1	T_{RCT}	10.0		7.5		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0	ns
Read Operation, Clocking Data into Flip-Flop							
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		ns
Read During Write							
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop							
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		ns
	32 x 1	T_{WCKT}	15.0		12.0		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Inputs

Description	Symbol	-6		-5		Units
		Min	Max	Min	Max	
Propagation Delays from CMOS or TTL Levels Pad to I1, I2	T_{PID}		4.0		3.0	ns

Outputs

Description	Symbol	-6		-5		Units
		Min	Max	Min	Max	
Propagation Delays to TTL Levels						
Output (O) to Pad (Resistive Mode)	T_{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T_{OPC}		10.5		8.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T_{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T_{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T_{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T_{TSONC}		16.0		12.0	ns
Propagation Delays to CMOS Levels						
Output (O) to Pad (Resistive Mode)	T_{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T_{OPC}		9.0		7.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T_{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T_{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T_{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T_{TSONC}		14.0		11.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

2. Output delays change with capacitive loading as described in the following table.

	TTL Levels	CMOS Levels	Units
Resistive Mode	0.03	0.03	ns/pF
Capacitive Mode	0.04	0.03	ns/pF

3. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor, or alternatively, configured as a driven output or be driven from an external source.

XC4003H Pinouts

Pin Description	PG191	PQ208	Bound Scan
VCC	J4	183	–
I/O (A8)	J3	184	62
I/O (A9)	J2	185	65
I/O	J1	186	68
I/O	H1	187	71
I/O	H2	188	74
I/O	H3	189	77
I/O (A10)	G1	190	80
I/O (A11)	G2	191	83
I/O	F1	192	86
I/O	E1	193	89
GND	G3	194	–
I/O	F2	195	92
I/O	D1	196	95
I/O	C1	197	98
I/O	E2	198	101
I/O (A12)	F3	199	104
I/O (A13)	D2	200	107
I/O	B1	201	110
I/O	E3	202	113
I/O (A14)	C2	203	116
SGCK1 (A15, I/O)	B2	204	119
VCC	D3	205	–
–	–	206*	–
–	–	207*	–
–	–	208*	–
–	–	1*	–
GND	D4	2	–
–	–	3*	–
PGCK1 (A16, I/O)	C3	4	122
I/O (A17)	C4	5	125
I/O	B3	6	128
I/O	C5	7	131
I/O (TDI)	A2	8	134
I/O (TCK)	B4	9	137
I/O	C6	10	140
I/O	A3	11	143
I/O	B5	12	146
I/O	B6	13	149
GND	C7	14	–
I/O	A4	15	152
I/O	A5	16	155
I/O (TMS)	B7	17	158
I/O	A6	18	161
I/O	C8	19	164
I/O	A7	20	167
I/O	B8	21	170
I/O	A8	22	173
I/O	B9	23	176
I/O	C9	24	179
GND	D9	25	–
VCC	D10	26	–

Pin Description	PG191	PQ208	Bound Scan
I/O	C10	27	182
I/O	B10	28	185
I/O	A9	29	188
I/O	A10	30	191
I/O	A11	31	194
I/O	C11	32	197
I/O	B11	33	200
I/O	A12	34	203
I/O	B12	35	206
I/O	A13	36	209
GND	C12	37	–
I/O	B13	38	212
I/O	A14	39	215
I/O	A15	40	218
I/O	C13	41	221
I/O	B14	42	224
I/O	A16	43	227
I/O	B15	44	230
I/O	C14	45	233
I/O	A17	46	236
SGCK2 (I/O)	B16	47	239
O (M1)	C15	48	242
GND	D15	49	–
I (M0)	A18	50	245†
–	–	51*	–
–	–	52*	–
–	–	53*	–
–	–	54*	–
VCC	D16	55	–
I (M2)	C16	56	246†
PGCK2 (I/O)	B17	57	247
I/O (HDC)	E16	58	250
I/O	C17	59	253
I/O	D17	60	256
I/O	B18	61	259
I/O (LDC)	E17	62	262
I/O	F16	63	265
I/O	C18	64	268
I/O	D18	65	271
I/O	F17	66	274
GND	G16	67	–
I/O	E18	68	277
I/O	F18	69	280
I/O	G17	70	283
I/O	G18	71	286
I/O	H16	72	289
I/O	H17	73	292
I/O	H18	74	295
I/O	J18	75	298
I/O	J17	76	301
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	J16	77	304
VCC	J15	78	–

Pin Description	PG191	PQ208	Bound Scan
GND	K15	79	–
I/O	K16	80	307
I/O	K17	81	310
I/O	K18	82	313
I/O	L18	83	316
I/O	L17	84	319
I/O	L16	85	322
I/O	M18	86	325
I/O	M17	87	328
I/O	N18	88	331
I/O	P18	89	334
GND	M16	90	–
I/O	N17	91	337
I/O	R18	92	340
I/O	T18	93	343
I/O	P17	94	346
I/O	N16	95	349
I/O	T17	96	352
I/O	R17	97	355
I/O	P16	98	358
I/O	U18	99	361
SGCK3 (I/O)	T16	100	364
GND	R16	101	–
–	–	102*	–
DONE	U17	103	–
–	–	104*	–
–	–	105*	–
VCC	R15	106	–
–	–	107*	–
PROG	V18	108	–
I/O (D7)	T15	109	367
PGCK3 (I/O)	U16	110	370
I/O	T14	111	373
I/O	U15	112	376
I/O (D6)	V17	113	379
I/O	V16	114	382
I/O	T13	115	385
I/O	U14	116	388
I/O	V15	117	391
I/O	V14	118	394
GND	T12	119	–
I/O	U13	120	397
I/O	V13	121	400
I/O (D5)	U12	122	403
I/O (CS0)	V12	123	406
I/O	T11	124	409
I/O	U11	125	412
I/O	V11	126	415
I/O	V10	127	418
I/O (D4)	U10	128	421
I/O	T10	129	424
VCC	R10	130	–

Pin Description	PG191	PQ208	Bound Scan
GND	R9	131	–
I/O (D3)	T9	132	427
I/O ($\overline{\text{RS}}$)	U9	133	430
I/O	V9	134	433
I/O	V8	135	436
I/O	U8	136	439
I/O	T8	137	442
I/O (D2)	V7	138	445
I/O	U7	139	448
I/O	V6	140	451
I/O	U6	141	454
GND	T7	142	–
I/O	V5	143	457
I/O	V4	144	460
I/O	U5	145	463
I/O	T6	146	466
I/O (D1)	V3	147	469
I/O (RCLK-$\overline{\text{BUSY}}$/ RDY)	V2	148	472
I/O	U4	149	475
I/O	T5	150	478
I/O (D0, DIN)	U3	151	481
SGCK4 (DOUT, I/O)	T4	152	484
CCLK	V1	153	–
VCC	R4	154	–
–	–	155*	–
–	–	156*	–
–	–	157*	–
–	–	158*	–
O (TDO)	U2	159	–
GND	R3	160	–
I/O (A0, $\overline{\text{WS}}$)	T3	161	2
PGCK4 (I/O, A1)	U1	162	5
I/O	P3	163	8
I/O	R2	164	11
I/O (CS1, A2)	T2	165	14
I/O (A3)	N3	166	17
I/O	P2	167	20
I/O	T1	168	23
I/O	R1	169	26
I/O	N2	170	29
GND	M3	171	–
I/O	P1	172	32
I/O	N1	173	35
I/O (A4)	M2	174	38
I/O (A5)	M1	175	41
I/O	L3	176	44
I/O	L2	177	47
I/O	L1	178	50
I/O	K1	179	53
I/O (A6)	K2	180	56
I/O (A7)	K3	181	59
GND	K4	182	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCANT.UPD

XC4005H Pinouts

Pin Description	PG223	MQ240	Bound Scan
VCC	J4	212	–
I/O (A8)	J3	213	74
I/O (A9)	J2	214	77
I/O	J1	215	80
I/O	H1	216	83
I/O	H2	217	86
I/O	H3	218	89
GND	–	219	–
I/O (A10)	G1	220	92
I/O (A11)	G2	221	95
VCC	–	222	–
I/O	H4	223	98
I/O	G4	224	101
I/O	F1	225	104
I/O	E1	226	107
GND	G3	227	–
I/O	F2	228	110
I/O	D1	229	113
I/O	C1	230	116
I/O	E2	231	119
I/O (A12)	F3	232	122
I/O (A13)	D2	233	125
I/O	F4	234	128
I/O	E4	235	131
I/O	B1	236	134
I/O	E3	237	137
I/O (A14)	C2	238	140
SGCK1 (A15, I/O)	B2	239	143
VCC	D3	240	–
GND	D4	1	–
PGCK1 (A16,I/O)	C3	2	146
I/O (A17)	C4	3	149
I/O	B3	4	152
I/O	C5	5	155
I/O (TDI)	A2	6	158
I/O (TCK)	B4	7	161
I/O	C6	8	164
I/O	A3	9	167
I/O	B5	10	170
I/O	B6	11	173
I/O	D5	12	176
I/O	D6	13	179
GND	C7	14	–
I/O	A4	15	182
I/O	A5	16	185
I/O (TMS)	B7	17	188
I/O	A6	18	191
VCC	–	19	–
I/O	D7	20	194
I/O	D8	21	197
GND	–	22	–
I/O	C8	23	200
I/O	A7	24	203
I/O	B8	25	206
I/O	A8	26	209
I/O	B9	27	212
I/O	C9	28	215
GND	D9	29	–
VCC	D10	30	–
I/O	C10	31	218

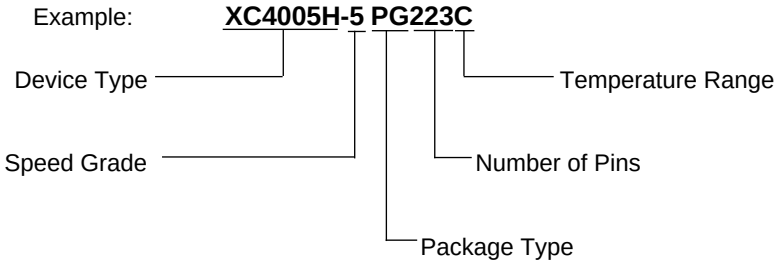
Pin Description	PG223	MQ240	Bound Scan
I/O	B10	32	221
I/O	A9	33	224
I/O	A10	34	227
I/O	A11	35	230
I/O	C11	36	233
GND		37	
I/O	D11	38	236
I/O	D12	39	239
VCC	–	40	–
I/O	B11	41	242
I/O	A12	42	245
I/O	B12	43	248
I/O	A13	44	251
GND	C12	45	–
I/O	D13	46	254
I/O	D14	47	257
I/O	B13	48	260
I/O	A14	49	263
I/O	A15	50	266
I/O	C13	51	269
I/O	B14	52	272
I/O	A16	53	275
I/O	B15	54	278
I/O	C14	55	281
I/O	A17	56	284
SGCK2 (I/O)	B16	57	287
O (M1)	C15	58	290
GND	D15	59	–
I (M0)	A18	60	293†
VCC	D16	61	–
I (M2)	C16	62	294†
PGCK2 (I/O)	B17	63	295
I/O (HDC)	E16	64	298
I/O	C17	65	301
I/O	D17	66	304
I/O	B18	67	307
I/O (LDC)	E17	68	310
I/O	F16	69	313
I/O	C18	70	316
I/O	D18	71	319
I/O	F17	72	322
I/O	E15	73	325
I/O	F15	74	328
GND	G16	75	–
I/O	E18	76	331
I/O	F18	77	334
I/O	G17	78	337
I/O	G18	79	340
VCC	–	80	–
I/O	H16	81	343
I/O	H17	82	346
GND	–	83	–
I/O	G15	84	349
I/O	H15	85	352
I/O	H18	86	355
I/O	J18	87	358
I/O	J17	88	361
I/O ($\overline{ERR}$, $\overline{INIT}$)	J16	89	364
VCC	J15	90	–
GND	K15	91	–

Pin Description	PG223	MQ240	Bound Scan
I/O	K16	92	367
I/O	K17	93	370
I/O	K18	94	373
I/O	L18	95	376
I/O	L17	96	379
I/O	L16	97	382
GND	–	98	–
I/O	L15	99	385
I/O	M15	100	388
VCC	-	101	–
I/O	M18	102	391
I/O	M17	103	394
I/O	N18	104	397
I/O	P18	105	400
GND	M16	106	–
I/O	N15	107	403
I/O	P15	108	406
I/O	N17	109	409
I/O	R18	110	412
I/O	T18	111	415
I/O	P17	112	418
I/O	N16	113	421
I/O	T17	114	424
I/O	R17	115	427
I/O	P16	116	430
I/O	U18	117	433
SGCK3 (I/O)	T16	118	436
GND	R16	119	–
DONE	U17	120	–
VCC	R15	121	–
$\overline{PROG}$	V18	122	–
I/O (D7)	T15	123	439
PGCK3 (I/O)	U16	124	442
I/O	T14	125	445
I/O	U15	126	448
I/O	R14	127	451
I/O	R13	128	454
I/O (D6)	V17	129	457
I/O	V16	130	460
I/O	T13	131	463
I/O	U14	132	466
I/O	V15	133	469
I/O	V14	134	472
GND	T12	135	–
I/O	R12	136	475
I/O	R11	137	478
I/O	U13	138	481
I/O	V13	139	484
VCC	–	140	–
I/O (D5)	U12	141	487
I/O ($\overline{CSO}$)	V12	142	490
GND	–	143	–
I/O	T11	144	493
I/O	U11	145	496
I/O	V11	146	499
I/O	V10	147	502
I/O (D4)	U10	148	505
I/O	T10	149	508
VCC	R10	150	–
GND	R9	151	–

Pin Description	PG223	MQ240	Bound Scan
I/O (D3	T9	152	511
I/O (RS)	U9	153	514
I/O	V9	154	517
I/O	V8	155	520
I/O	U8	156	523
I/O	T8	157	526
GND		158	
I/O (D2)	V7	159	529
I/O	U7	160	532
VCC	–	161	–
I/O	V6	162	535
I/O	U6	163	538
I/O	R8	164	541
I/O	R7	165	544
GND	T7	166	–
I/O	R6	167	547
I/O	R5	168	550
I/O	V5	169	553
I/O	V4	170	556
I/O	U5	171	559
I/O	T6	172	562
I/O (D1)	V3	173	565
I/O (RCLK-$\overline{BUSY}$/ RDY)	V2	174	568
I/O	U4	175	571
I/O	T5	176	574
I/O (D0, DIN)	U3	177	577
SGCK4 (DOUT, I/O)	T4	178	580
CCLK	V1	179	–
VCC	R4	180	–
O (TDO)	U2	181	–
GND	R3	182	–
I/O (A0, $\overline{WS}$)	T3	183	2
PGCK4 (I/O, A1)	U1	184	5
I/O	P3	185	8
I/O	R2	186	11
I/O (CS1, A2)	T2	187	14
I/O (A3)	N3	188	17
I/O	P4	189	20
I/O	N4	190	23
I/O	P2	191	26
I/O	T1	192	29
I/O	R1	193	32
I/O	N2	194	35
–	–	195*	–
GND	M3	196	–
I/O	P1	197	38
I/O	N1	198	41
I/O	M4	199	44
I/O	L4	200	47
VCC	–	201	–
I/O (A4)	M2	202	50
I/O (A5)	M1	203	53
GND	–	204	–
I/O	L3	205	56
I/O	L2	206	59
I/O	L1	207	62
I/O	K1	208	65
I/O (A6)	K2	209	68
I/O (A7)	K3	210	71
GND	K4	211	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST. TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	METAL PQFP
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299
XC4003H	-6										C I		C I						
	-5										C		C						
XC4005H	-6														C I		C I	C I	
	-5														C		C	C	

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C

B = MIL-STD-883C Class B Parentheses indicate future product plans