



# STGB7NB40LZ

## N-CHANNEL CLAMPED 14A - D<sup>2</sup>PAK INTERNALLY CLAMPED PowerMESH™ IGBT

TYPE	V <sub>CES</sub>	V <sub>CE(sat)</sub>	I <sub>C</sub>
STGB7NB40LZ	CLAMPED	< 1.50 V	14 A

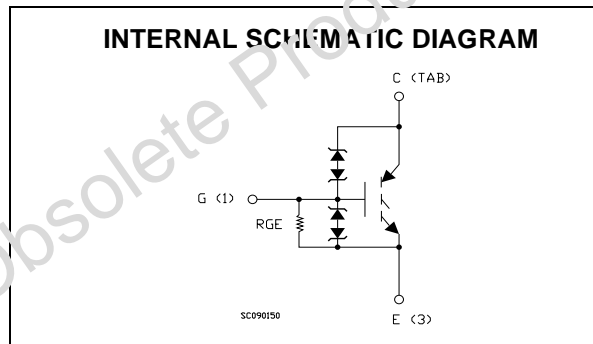
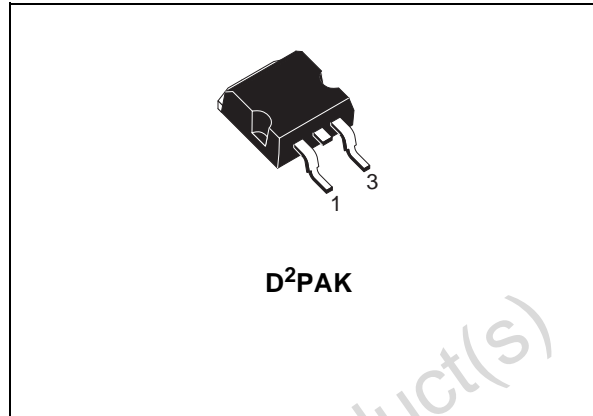
- POLYSILICON GATE VOLTAGE DRIVEN
- LOW THRESHOLD VOLTAGE
- LOW ON-VOLTAGE DROP
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- HIGH VOLTAGE CLAMPING FEATURE

### DESCRIPTION

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The built in collector-gate zener exhibits a very precise active clamping while the gate-emitter zener supplies an ESD protection.

### APPLICATIONS

- AUTOMOTIVE IGNITION



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Collector-Emitter Voltage (V <sub>GS</sub> = 0)	CLAMPED	V
V <sub>ECR</sub>	Reverse Battery Protection	20	V
V <sub>GE</sub>	Gate-Emitter Voltage	CLAMPED	V
I <sub>C</sub>	Collector Current (continuous) at 100°C	14	A
R <sub>G</sub>	Minimum External Gate Resistor	500	Ω
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	100	W
	Derating Factor	0.66	W/°C
E <sub>CL</sub>	Single Pulse Collector to Emitter Avalanche Energy I <sub>C</sub> = 13 A ; T <sub>j</sub> = 150°C (see fig.1-2)	130	mJ
E <sub>ECAV</sub>	Reverse Avalanche Energy I <sub>C</sub> = 7 A ; f = 100 Hz ; T <sub>C</sub> = 25°C	10	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Operating Junction Temperature		

## STGB7NB40LZ

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (free air)	62.5	°C/W

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25°C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>(CES)</sub>	Collector-Emitter Clamped Voltage	I <sub>C</sub> = 10 mA, V <sub>GE</sub> = 0, T <sub>C</sub> = -40°C to 150°C; R <sub>G</sub> = 1 KΩ	370	400	430	V
BV <sub>(ECS)</sub>	Emitter Collector Break-down Voltage	I <sub>EC</sub> = 75 mA, V <sub>GE</sub> = 0,	20	27		V
BV <sub>GE</sub>	Gate Emitter Break-down Voltage	I <sub>G</sub> = ± 2 mA	12		16	V
I <sub>CES</sub>	Collector-Emitter Leakage Current	V <sub>GE</sub> = 200 V, V <sub>CE</sub> = 0, R <sub>G</sub> = 1 KΩ T <sub>C</sub> = 25°C T <sub>C</sub> = 150°C			25 250	μA μA
I <sub>GES</sub>	Gate-Emitter Leakage Current (V <sub>CE</sub> = 0)	V <sub>GE</sub> = ± 10 V, V <sub>CE</sub> = 0			1000	μA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GE(th)</sub>	Gate Threshold Voltage	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1 mA, T <sub>C</sub> = 25°C V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1 mA, T <sub>C</sub> = 150°C	1.2 0.75		2.2 1.8	V V
V <sub>CE(SAT)</sub>	Collector-Emitter Saturation Voltage	V <sub>GE</sub> = 4.5 V, I <sub>C</sub> = 7 A, T <sub>J</sub> = 25°C V <sub>GE</sub> = 5.0 V, I <sub>C</sub> = 14 A, T <sub>C</sub> = 25°C		1.3	1.50 1.9	V V
R <sub>GE</sub>	Gate Emitter Resistance		10	20	30	KΩ

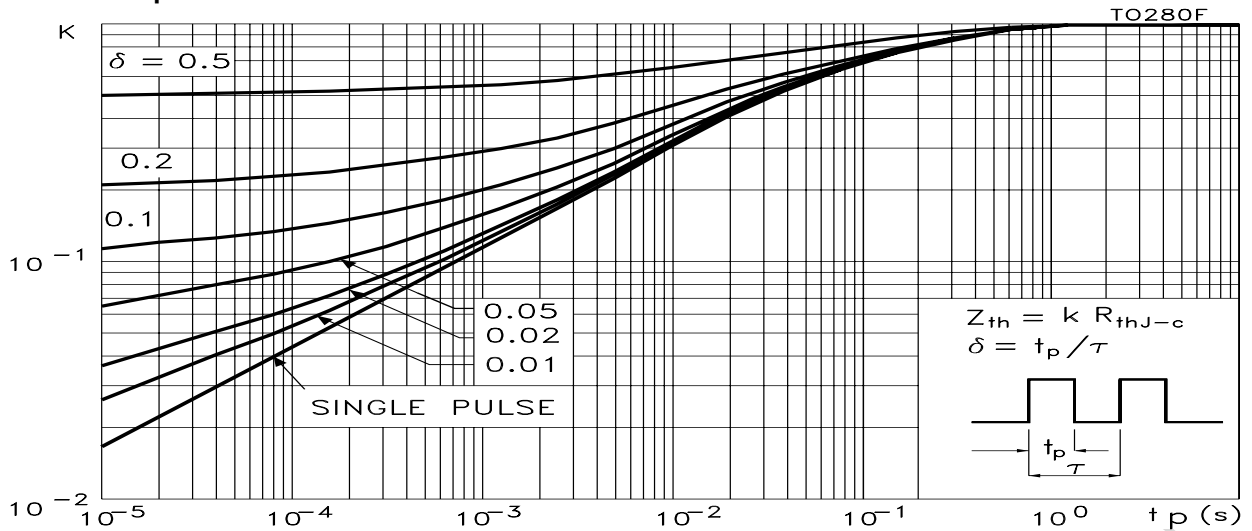
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C <sub>ies</sub>	Input Capacitance	V <sub>CE</sub> = 25 V, f = 1 MHz, V <sub>GE</sub> = 0		910		pF
C <sub>oes</sub>	Output Capacitance			80		pF
C <sub>res</sub>	Reverse Transfer Capacitance			15		pF
Q <sub>g</sub>	Gate Charge	V <sub>CE</sub> = 40 V, I <sub>C</sub> = 7 A, V <sub>GE</sub> = 5 V		22		nC

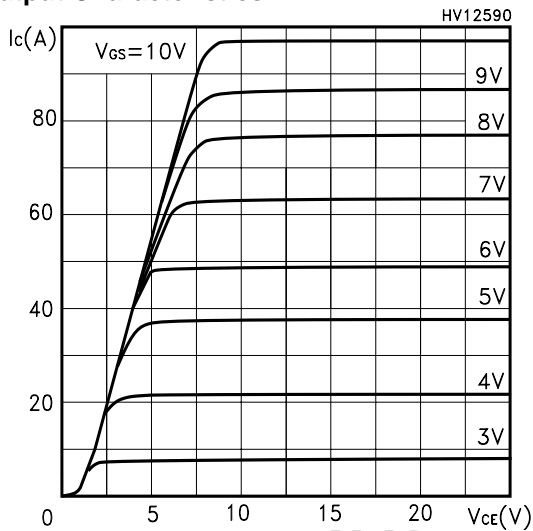
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Delay Time Current Rise Time	V <sub>CE</sub> = 14 V, R <sub>G</sub> = 1KΩ, R <sub>L</sub> = 1Ω, V <sub>GE</sub> = 5 V		0.9 4.5		μs μs
t <sub>d(off)</sub> t <sub>f</sub>	Delay Time Current Fall Time	V <sub>CE</sub> = 300 V, R <sub>G</sub> = 1KΩ, R <sub>L</sub> = 46Ω, V <sub>GE</sub> = 5 V		4.4 3.6		μs μs

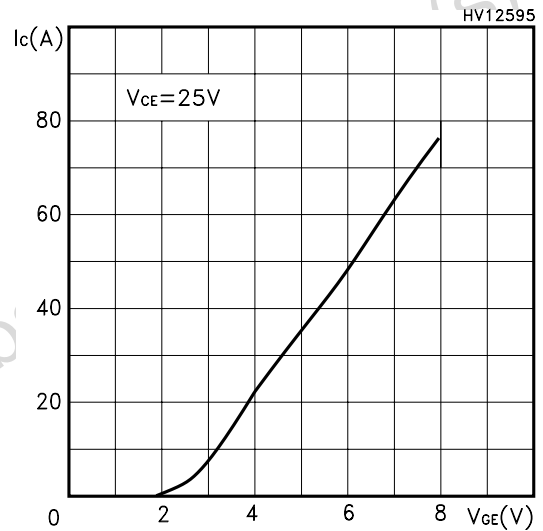
Thermal Impedance



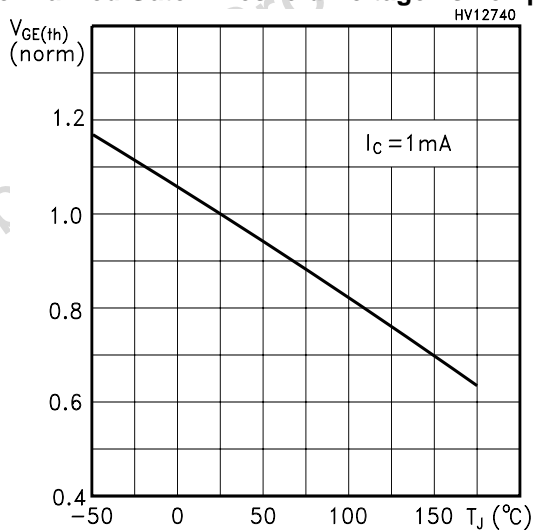
Output Characteristics



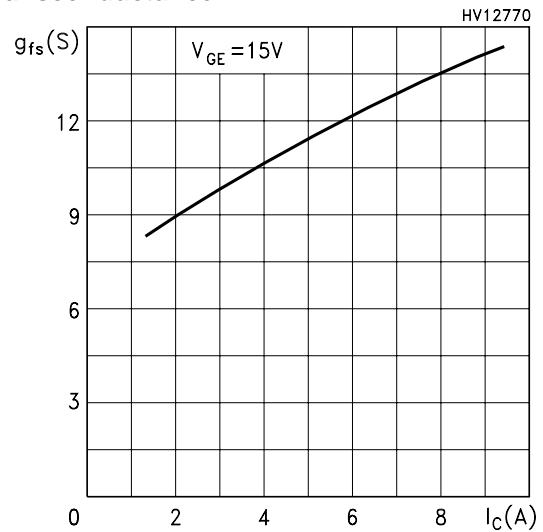
Transfer Characteristics



Normalized Gate Threshold Voltage vs Temp.

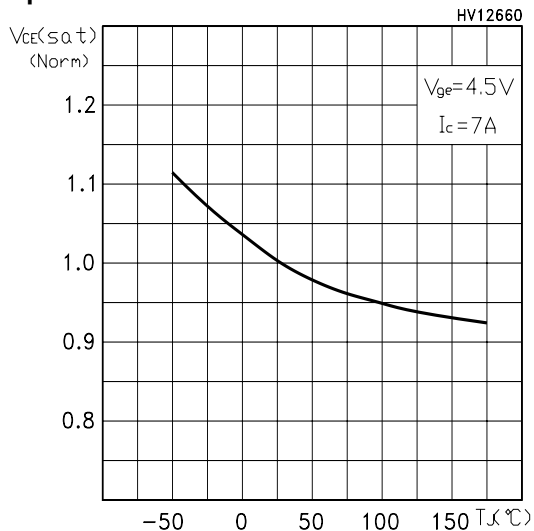


Transconductance

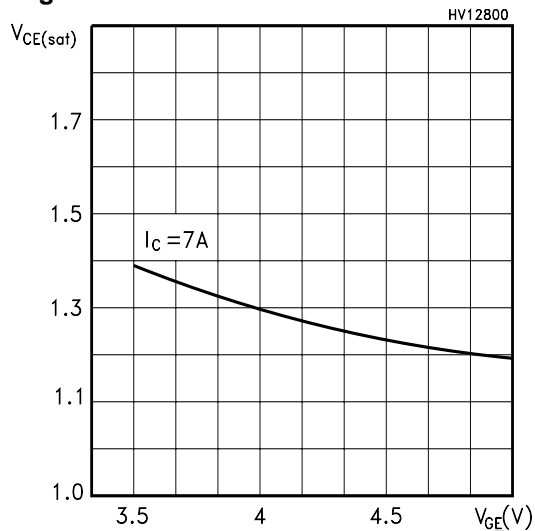


# STGB7NB40LZ

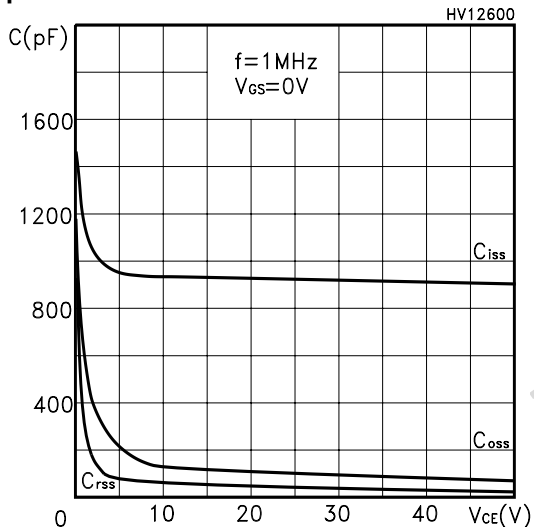
**Normalized Collector-Emitter On Voltage vs Temperature**



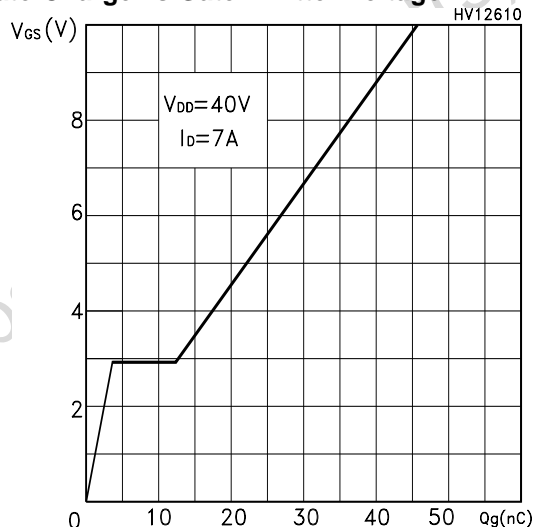
**Collector-Emitter On Voltage vs Gate-Emitter Voltage**



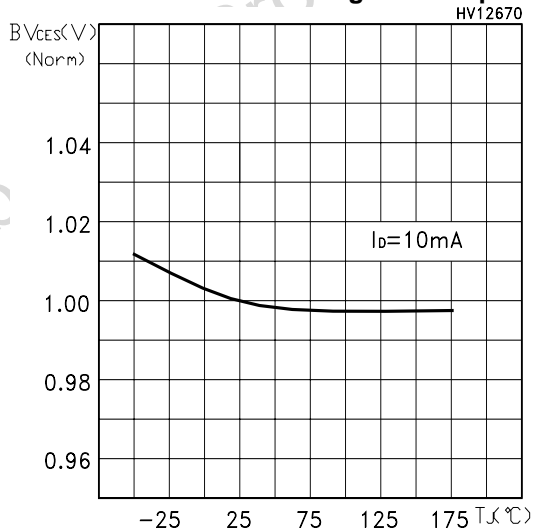
**Capacitance Variations**



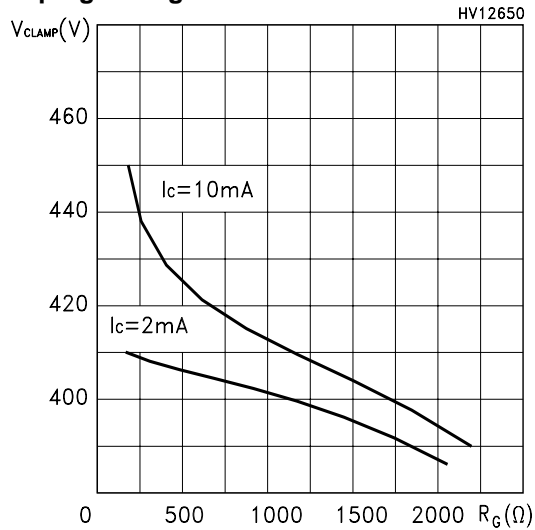
**Gate-Charge vs Gate-Emitter Voltage**



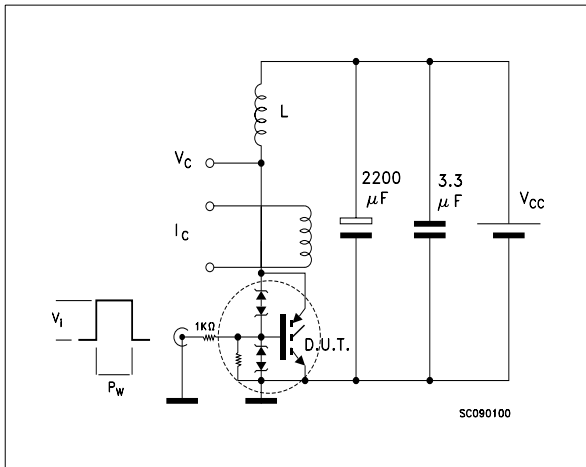
**Normalized Break-down Voltage vs Temp.**



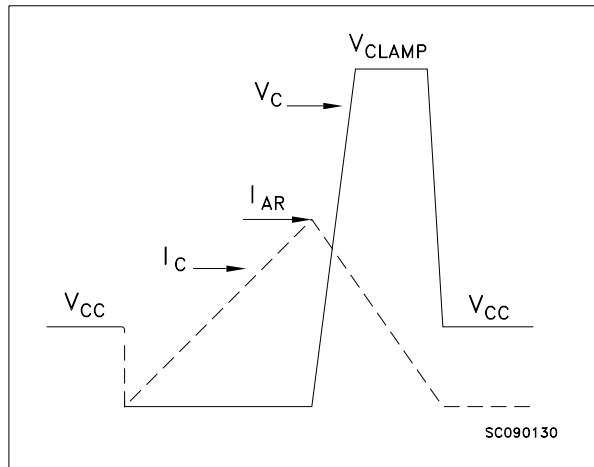
**Clamping Voltage vs Gate Resistance**



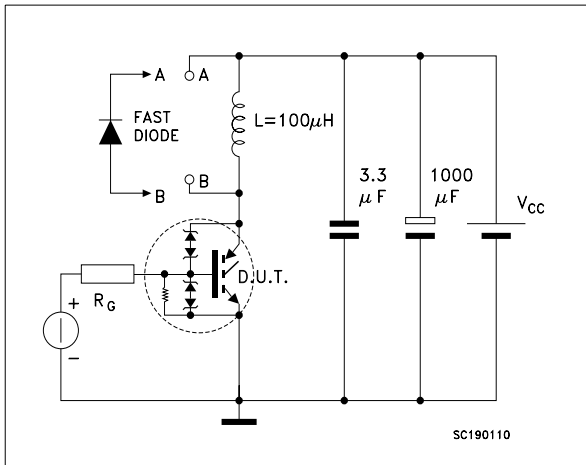
**Fig. 1: Unclamped Inductive Load Test Circuit**



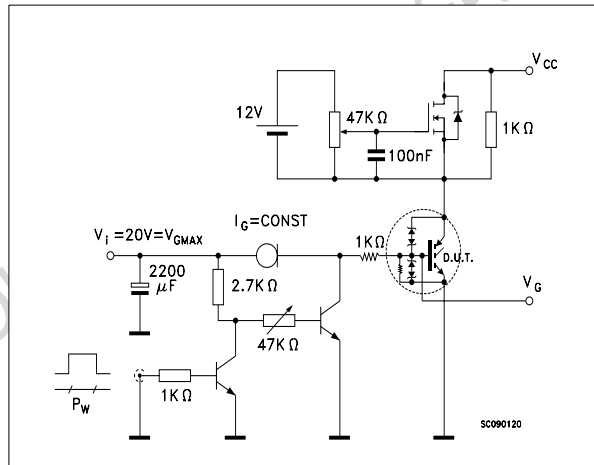
**Fig. 2: Unclamped Inductive Waveform**



**Fig. 3: Test Circuit For Inductive Load Switching And Diode Recovery Times**



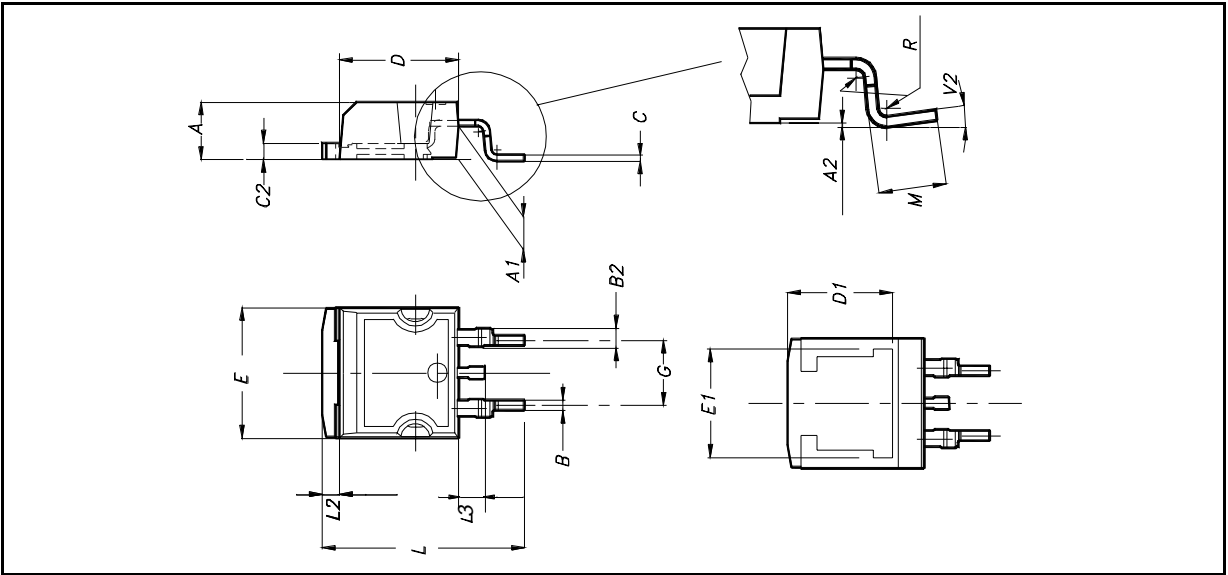
**Fig. 4: Gate Charge test Circuit**



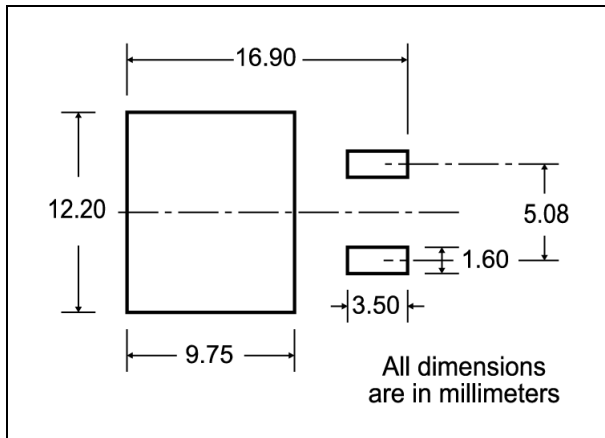
Obsolete Product

**D<sup>2</sup>PAK MECHANICAL DATA**

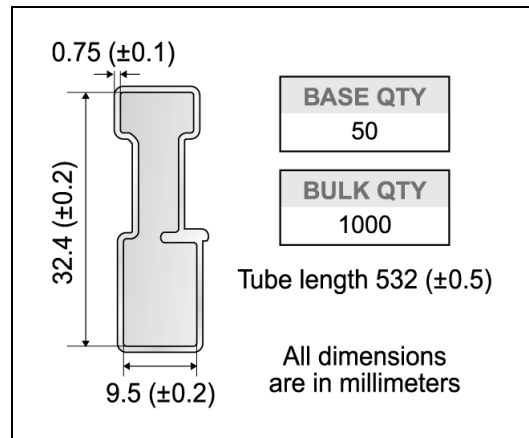
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



**D<sup>2</sup>PAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

<b>BASE QTY</b>	1000
<b>BULK QTY</b>	1000

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