Features

- **Single Supply Voltage Range, 2.7V to 3.6V**
- **Single Supply for Read and Write**
- **Fast Read Access Time – 90 ns**
- **Internal Program Control and Timer**
- **8K Bytes Boot Block with Lockout**
- **Fast Erase Cycle Time – 10 Seconds**
- **Byte-by-byte Programming – 30 µs/Byte Typical**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Program Detection**
- **Low Power Dissipation**
  - **25 mA Active Current**
  - **50 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**
- **Green (Pb/Halide-free) Packaging Option**

512K (64K x 8) Single 2.7-volt Battery-Voltage Flash Memory

AT49BV512

1. Description

The AT49BV512 is a 3-volt only, 512K Flash memories organized as 65,536 words of 8 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 90 ns with power dissipation of just 90 mW over the commercial temperature range. When the devices are deselected, the CMOS standby current is less than 50 µA.

To allow for simple in-system reprogrammability, the AT49BV512 does not require high input voltages for programming. Three-volt only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49BV512 is performed by erasing the entire 1 megabit of memory and then programming on a byte-by-byte basis. The typical byte programming time is a fast 30 µs. The end of a program cycle can be optionally detected by the $\overline{\text{DATA}}$ polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

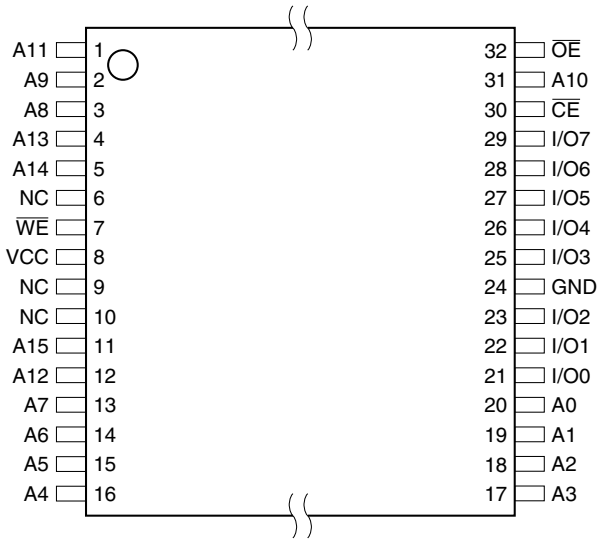
The optional 8K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

1026G–FLASH–10/05

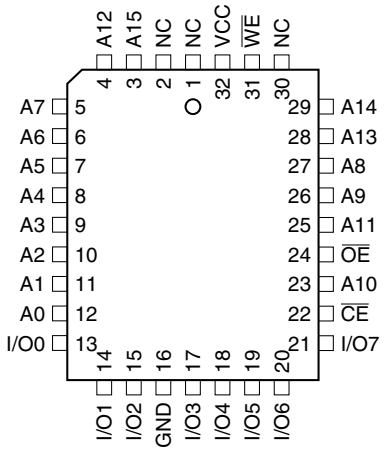
2. Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

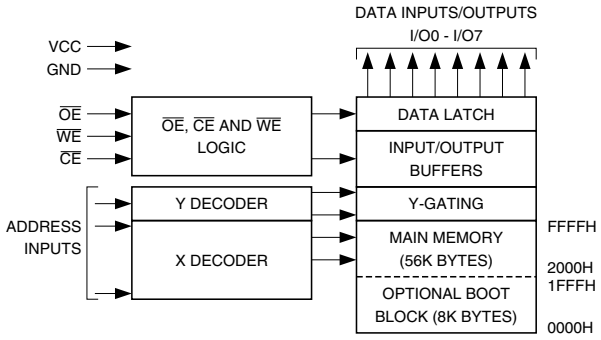
2.1 32VSOP/32TSOP (Type 1) Top View



2.2 32PLCC Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT49BV512 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Erasure

Before a byte can be reprogrammed, the 64K bytes memory array (or 56K bytes if the boot block featured is used) must be erased. The erased state of the memory bits is a logical “1”. The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

4.3 Byte Programming

Once the memory array is erased, the device is programmed (to a logical “0”) on a byte-by-byte basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

4.4 Boot Block Programming Lockout

The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have

to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 0000H to 1FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the "Command Definition Table" on page 5.

4.4.1 Boot Block Lockout Detection

A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry/Exit sections on page 12) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

4.5 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see "Operating Modes" on page 6 (for hardware operation) or Software Product Identification Entry/Exit sections on page 12. The manufacturer and device code is the same for both modes.

4.6 Data Polling

The AT49BV512 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

4.7 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling the AT49BV512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.8 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT49BV512 in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: Pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

4.9 Input Levels

While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$ and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

5. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout[1]	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[2]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[2]	1	XXXX	F0										

Notes: 1. The 8K byte boot sector has the address range 0000H to 1FFFH.
2. Either one of the Product ID exit commands can be used.

6. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. DC and AC Operating Range

		AT49BV512-90	AT49BV512-12
Operating Temperature (Case)	Com.		0°C - 70°C
	Ind.	-40°C - 85°C	
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V

8. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H,[3], A0 = V_{IL}	Manufacturer Code[4]
				A1 - A15 = V_{IL}, A9 = V_H,[3], A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}, A1 - A15 = V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}, A1 - A15 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 03H.
5. See details under Software Product Identification Entry/Exit sections on page 12.

9. DC Characteristics

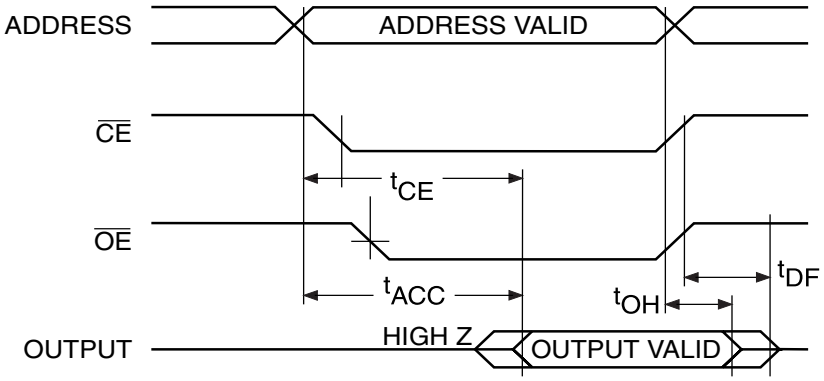
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		25	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V	2.4		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

10. AC Read Characteristics

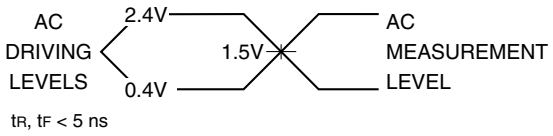
Symbol	Parameter	AT49BV512-90		AT49BV512-12		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE} [1]	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE} [2]	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF} [3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

11. AC Read Waveforms[1][2][3][4]

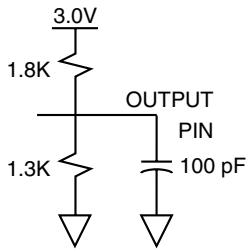


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL - 5 pF).
4. This parameter is characterized and is not 100% tested.

12. Input Test Waveforms and Measurement Level



13. Output Test Load



14. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

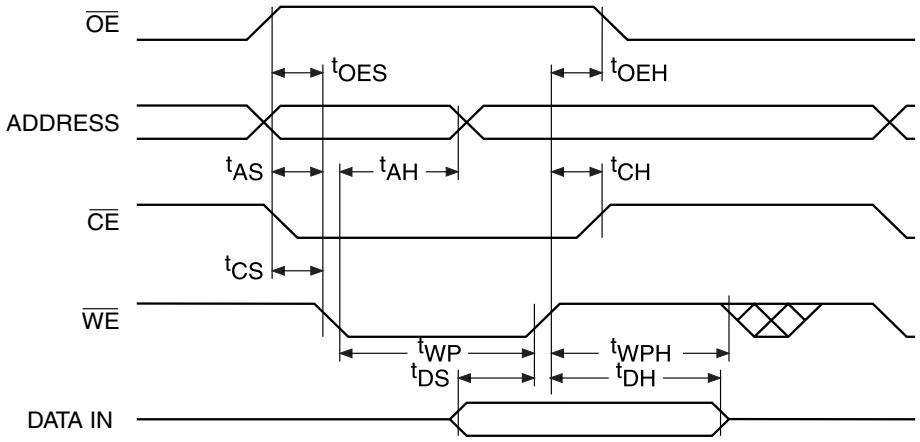
Note: 1. This parameter is characterized and is not 100% tested.

15. AC Byte Load Characteristics

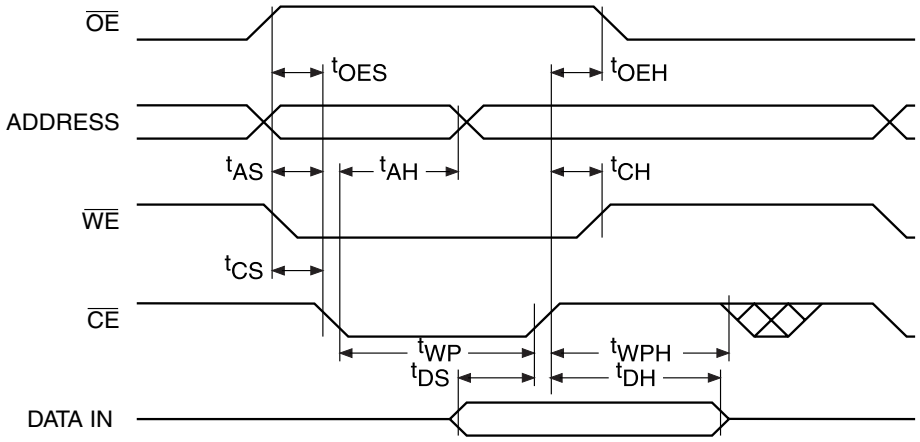
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	200		ns

16. AC Byte Load Waveforms

16.1 $\overline{WE}$ Controlled



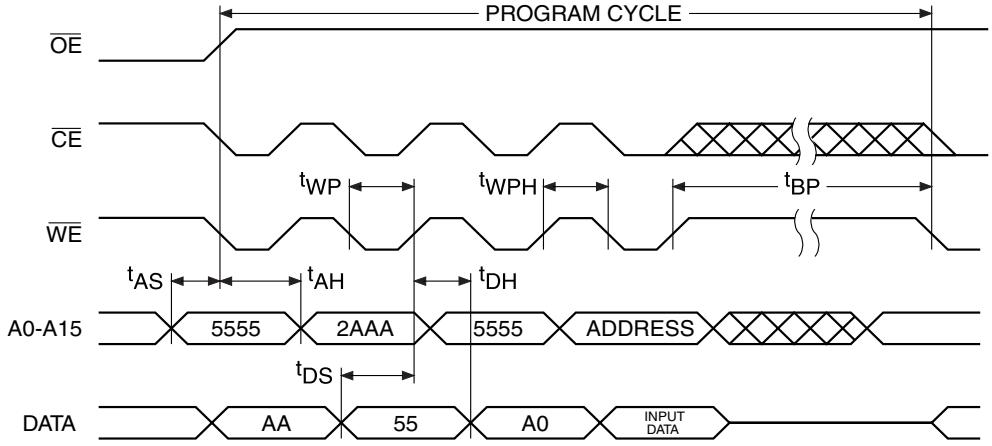
16.2 $\overline{CE}$ Controlled



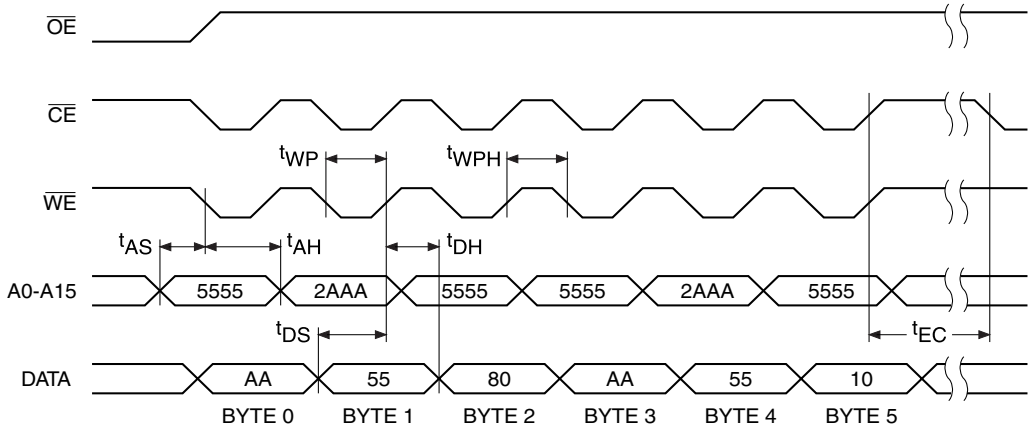
17. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		30		µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{DS}	Data Set-up Time	100			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	200			ns
t_{WPH}	Write Pulse Width High	200			ns
t_{EC}	Erase Cycle Time			10	seconds

18. Program Cycle Waveforms



19. Chip Erase Cycle Waveforms



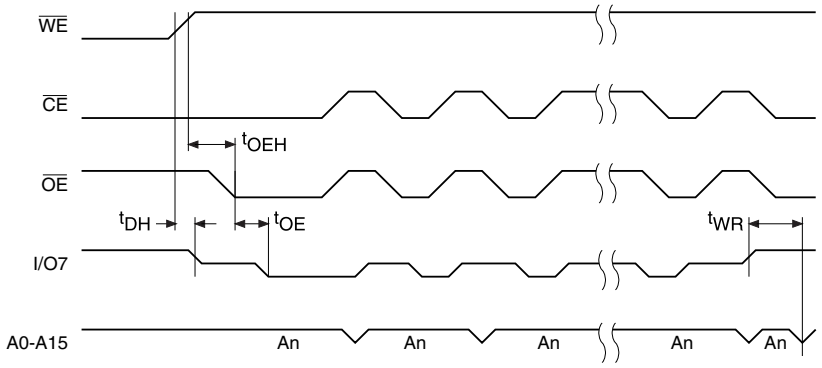
Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

20. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

21. $\overline{\text{Data}}$ Polling Waveforms

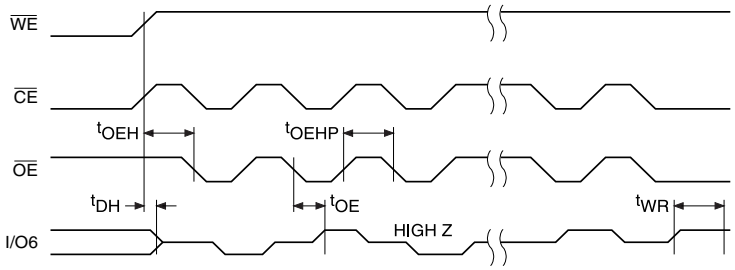


22. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

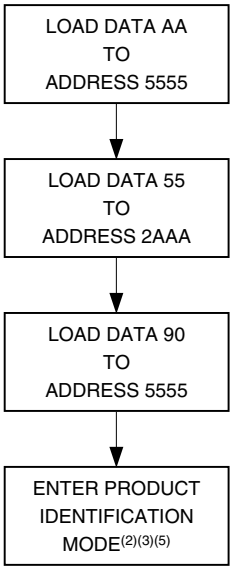
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

23. Toggle Bit Waveforms[1][2][3]

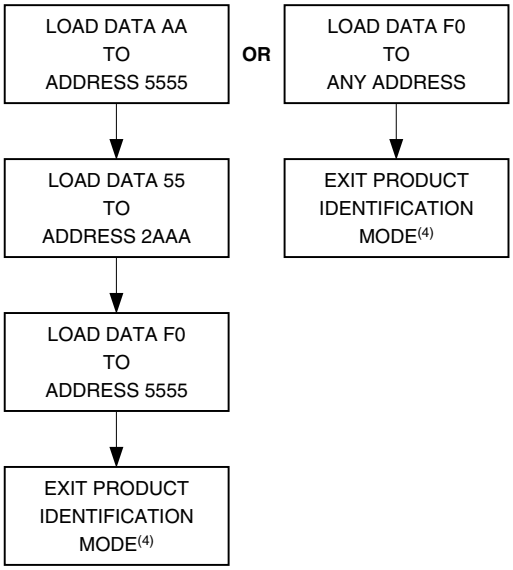


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

24. Software Product Identification Entry[1]

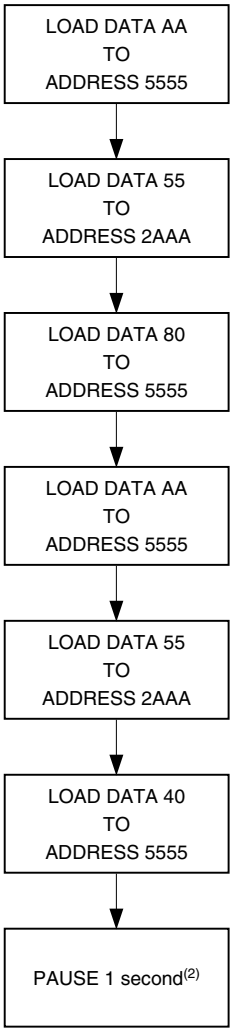


25. Software Product Identification Exit[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does note remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturers Code: 1FH
   Device Code: 03H.

26. Boot Block Lockout Feature Enable Algorithm[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

27. Ordering Information

27.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.05	AT49BV512-12JC	32J	Commercial (0°C - 70°C)

27.2 Green Package (Pb/Halide-free)

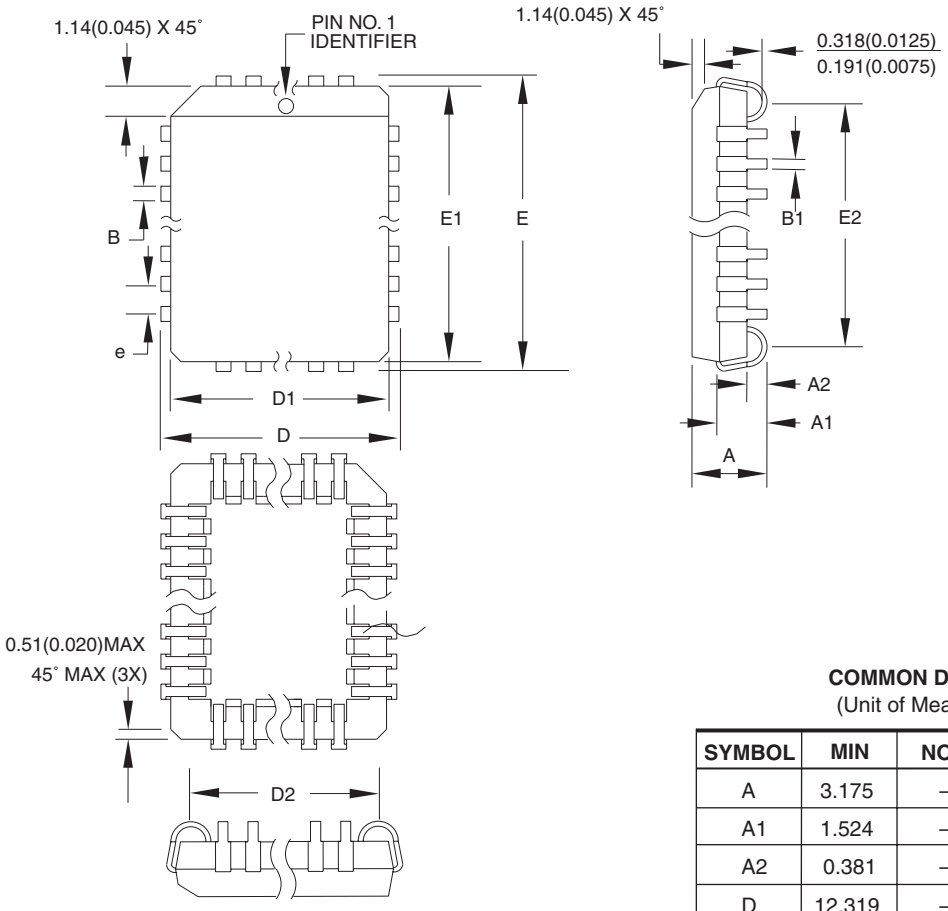
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	25	0.05	AT49BV512-90JU AT49BV512-90TU AT49BV512-90VU	32J 32T 32V	Industrial (-40°C - 85°C)

Note: 1. The AT49BV512 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 0000H to 1FFFH). Users requiring boot block protection to be in the higher address range should contact Atmel.

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier Package (PLCC)
32T	32-lead, Thin Small Outline Package (TSOP) (8 x 20 mm)
32V	32-lead, Thin Small Outline Package (VSOP) (8 x 14 mm)

28. Packaging Information

28.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

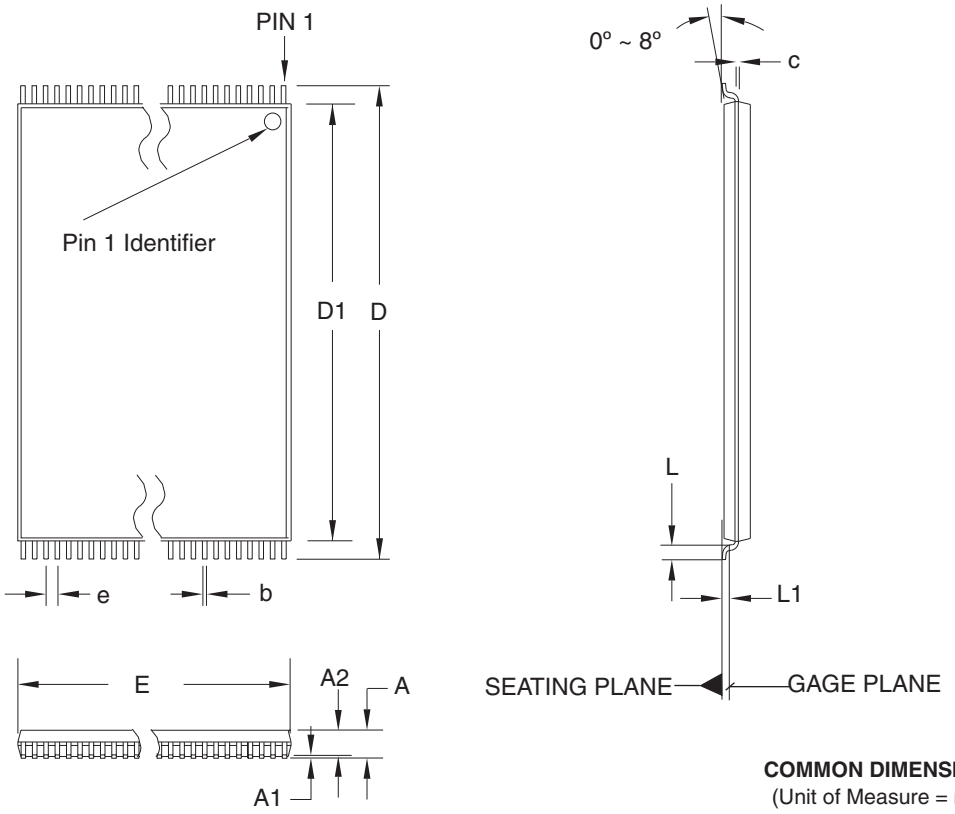
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

28.2 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

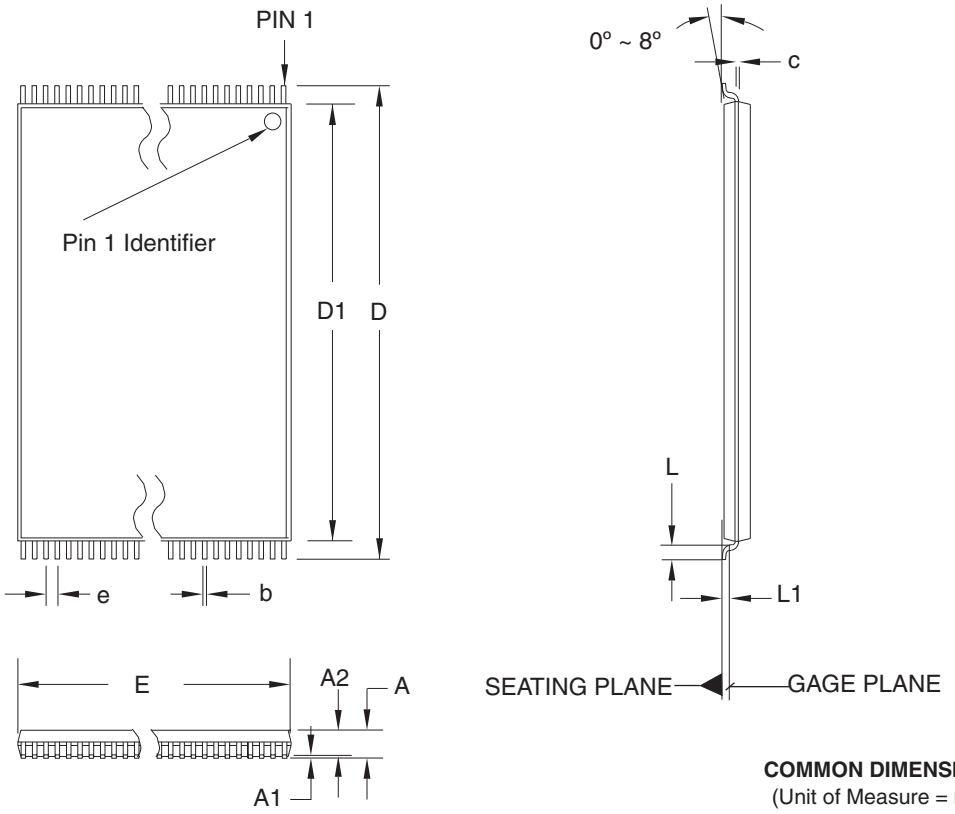
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

28.3 32V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	13.80	14.00	14.20	
D1	12.30	12.40	12.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BA.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32V**, 32-lead (8 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)	32V	B

29. Revision History

Revision No.	History
Revision F – August 2004	• Added a 55 ns speed option and removed the 90, 120, and 150 ns speed options for the die shrink redesign. The PDIP package was also eliminated. The die shrink redesign will have a marketing revision letter “A” marked after the date code on the topside of the device.
Revision G – Oct. 2005	• Added 120 ns PLCC commercial option. Added 90 ns Green option. Removed 55 ns speed option.

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