CY7B161
CY7B162

CYPRESS SEMICONDUCTOR

16K x 4 Static RAM Separate I/O

Features

- **Ultra high speed**
  - **— 8 ns t_{AA}**
- **Low active power**
  - **— 700 mW**
- **Low standby power**
  - **— 250 mW**
- **Transparent write (7B161)**
- **BiCMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

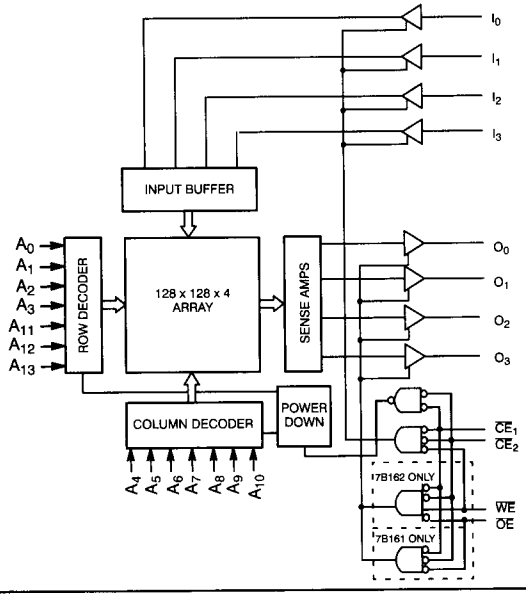
The CY7B161 and CY7B162 are high-performance BiCMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have a $\overline{CE}$ power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are all LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and $\overline{OE}$ LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The output pins remain in high-impedance state when write enable ($\overline{WE}$) is LOW (7B162 only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) is HIGH, or $\overline{OE}$ is HIGH.

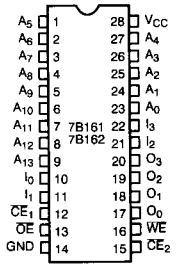
Logic Block Diagram



B161-1

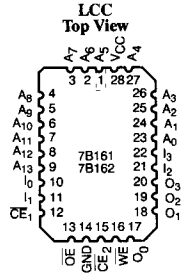
Pin Configurations

DIP/SOJ
Top View



B161-2

LCC
Top View



B161-3

Selection Guide

		7B161–8 7B162–8	7B161–10 7B162–10	7B161–12 7B162–12	7B161–15 7B162–15
Maximum Access Time (ns)		8	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	120	
	Military		145	140	135
Maximum Standby Current (mA)	Commercial	50	40	40	
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Latch-Up Current ..... > 200 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}	
		−8	−10, −12
Commercial	0°C to +70°C	5V ± 5%	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%	

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7B161−8 7B162−8 Min.	7B161−8 7B162−8 Max.	7B161−10 7B162−10 Min.	7B161−10 7B162−10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{max}.		Com'l		140		130	mA
				Mil				145	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3 V, I_{OUT} = 0 mA, Other Inputs = <0.8 or >3V, V_{CC}=Max.		Com'l		50		40	mA
				Mil				60	

Shaded area contains preliminary information.

Parameter	Description	Test Conditions			7B161−12 7B162−12 Min.	7B161−12 7B162−12 Max.	7B161−15 7B162−15 Min.	7B161−15 7B162−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{max}.		Com'l		120			mA
				Mil		140		135	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT}=0mA, Other Inputs = <0.8 or >3V, V_{CC}=Max.		Com'l		40			mA
				Mil		55		50	

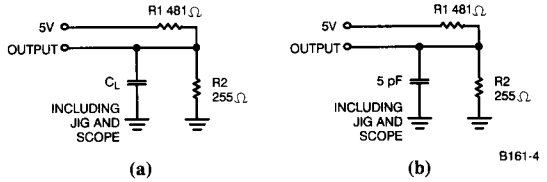
Capacitance[4]

Parameter	Description	Test Conditions	Max.[5]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

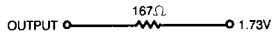
Notes:

1. V_{IL} (min.) = − 3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CerDIP (D22), which has maximums of C_{IN} = 9.5 pF and C_{OUT} = 9 pF.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6, 7]

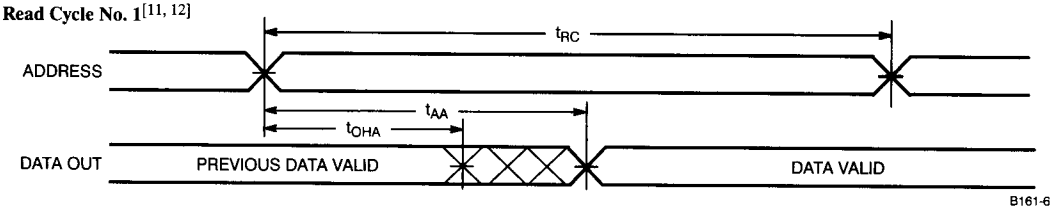
Parameter	Description	7B161–8 7B162–8		7B161–10 7B162–10		7B161–12 7B162–12		7B161–15 7B162–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Output Hold from Address Change	2.5		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4.2		5		6		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	1.5		2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	2		2		2		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		4		5		6		7	ns
WRITE CYCLE[10]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		8		10		ns
t_{AW}	Address Set-Up to Write End	7		8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6.5		8		8		10		ns
t_{SD}	Data Set-Up to Write End	4		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8] (7B162)	2		2		2		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9] (7B162)		4		5		6		7	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7B161)		8		10		12		15	ns
t_{ADV}	Data Valid to Output Valid (7B161)		8		10		12		15	ns

Notes:

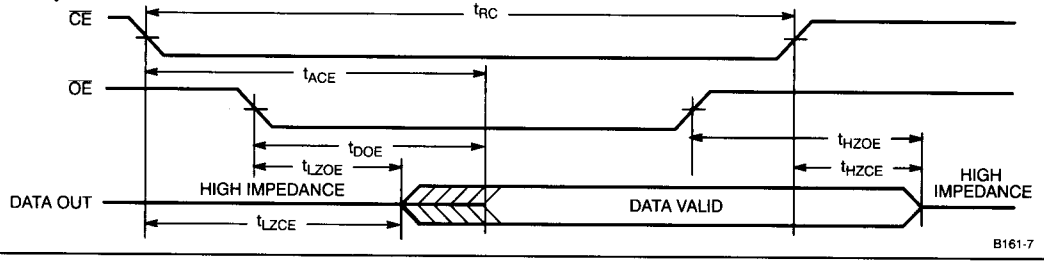
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and C_L = 20 pF.
7. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms section.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. This parameter is guaranteed and not 100% tested.
9. t_{HZCE}, t_{HZOE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage. This parameter is guaranteed and not 100% tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms[7]

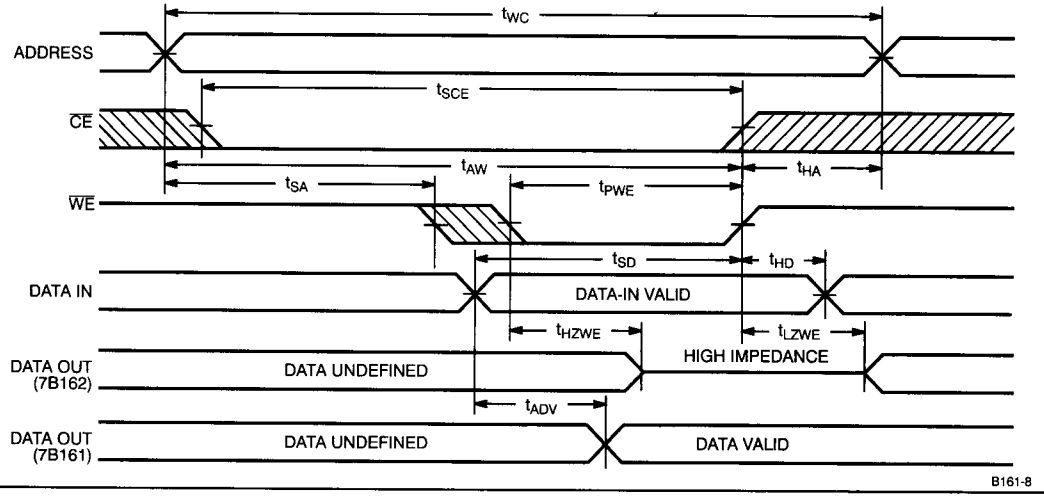
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



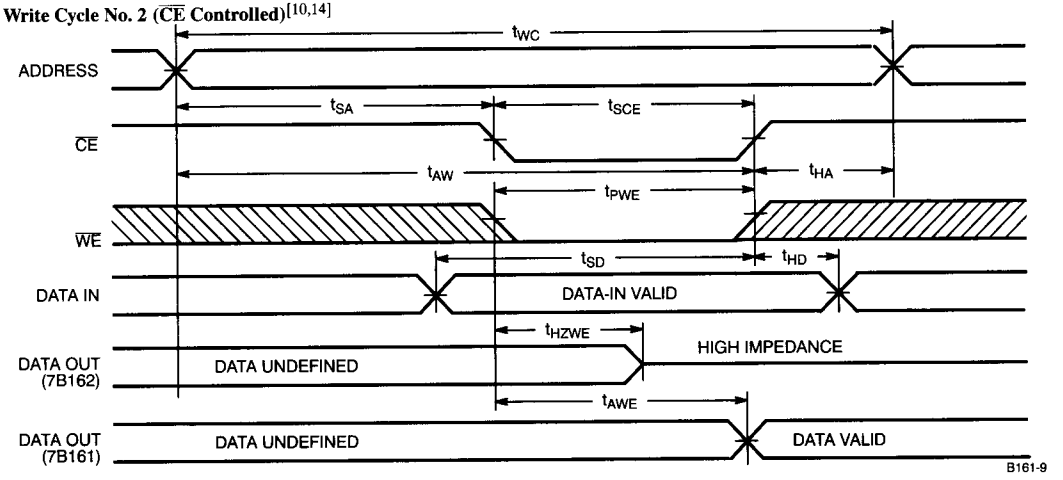
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2 \leq V_{IL}$. $\overline{OE} \leq V_{IL}$ also.
13. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.

Switching Waveforms[7] (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10,14]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7B162 only).

7B161 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Output	Input	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	L	Data In	Data In	Write
L	L	L	H	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

7B162 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Output	Input	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	X	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B161–8VC	V21	28-Lead Molded SOJ	
10	CY7B161–10DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B161–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B161–10VC	V21	28-Lead Molded SOJ	
	CY7B161–10DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B161–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B161–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B161–12VC	V21	28-Lead Molded SOJ	
	CY7B161–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B161–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B161–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B162–8VC	V21	28-Lead Molded SOJ	
10	CY7B162–10DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B162–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B162–10VC	V21	28-Lead Molded SOJ	
	CY7B162–10DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B162–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B162–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B162–12VC	V21	28-Lead Molded SOJ	
	CY7B162–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B162–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B162–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. 7B161 only.

Document #: 38-A-00014-E