



CYPRESS

CY7C161A  
CY7C162A

## 16K x 4 Static RAM with Separate I/O

### Features

- High speed  
— 20 ns  $t_{AA}$
- CMOS for optimum speed/power
- Transparent write (7C161A)
- Low active power  
— 550 mW
- Low standby power  
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

### Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

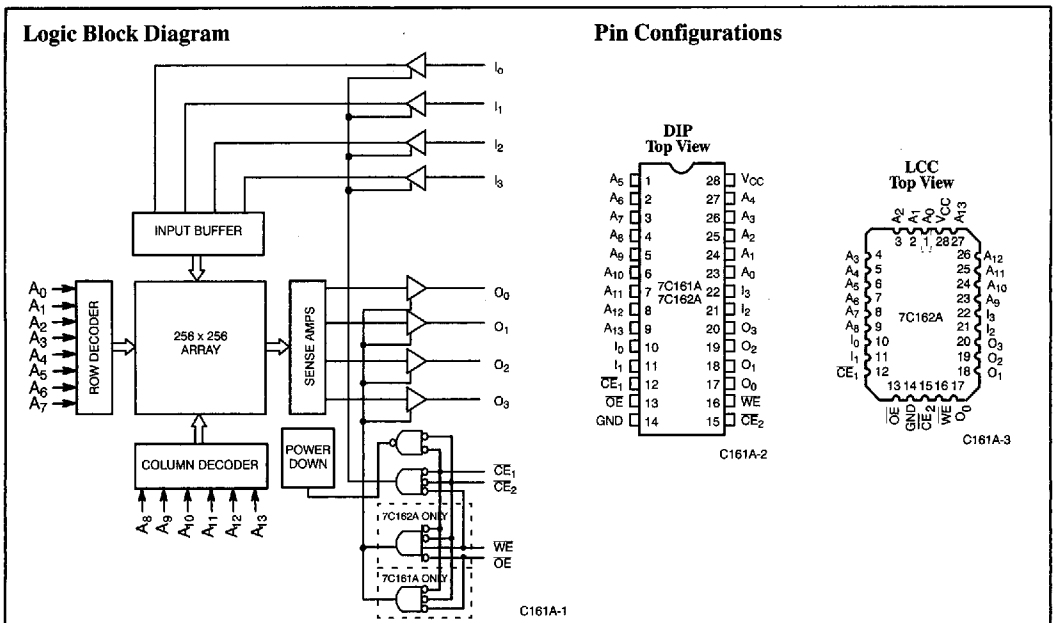
Writing to the device is accomplished when the chip enable ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input pins ( $I_0$  through  $I_3$ ) is written

into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) LOW while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ( $\overline{WE}$ ) is LOW (7C162A only), or one of the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) are HIGH.

A die coat is used to ensure alpha immunity.



### Selection Guide<sup>[1]</sup>

		7C161A-15 7C162A-15	7C161A-20 7C162A-20	7C161A-25 7C162A-25	7C161A-35 7C162A-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	100	100	100
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

### Note:

1. For commercial specifications, see the CY7C161/CY7C162 datasheet.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) .....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State <sup>[2]</sup> .....	-0.5V to +7.0V
DC Input Voltage <sup>[2]</sup> .....	-0.5V to +7.0V
Output Current into Outputs (LOW) .....	20 mA

 Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... &gt;200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Military <sup>[3]</sup>	-55°C to +125°C	5V ± 10%

**Notes:**

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- T<sub>A</sub> is the "instant on" case temperature.

**Electrical Characteristics Over the Operating Range<sup>[4]</sup>**

Parameter	Description	Test Conditions	7C161A-15 7C162A-15		7C161A-20 7C162A-20		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	Military	160		100	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%	Military	40		40	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Military	20		20	mA

Shaded area contains preliminary information.

**Electrical Characteristics Over the Operating Range<sup>[4]</sup> (continued)**

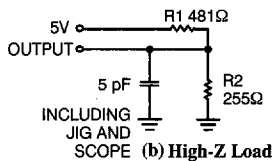
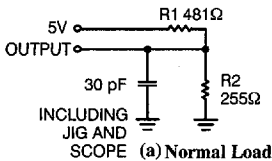
Parameter	Description	Test Conditions	7C161A-25 7C162A-25		7C161A-35 7C162A-35		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	Military	100		100	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%	Military	40		30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Military	20		20	mA

**Capacitance<sup>[6]</sup>**

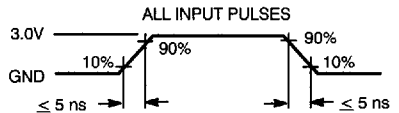
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

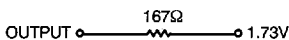
**AC Test Loads and Waveforms**


C161A-4



C161A-5

Equivalent to: THÉVENIN EQUIVALENT





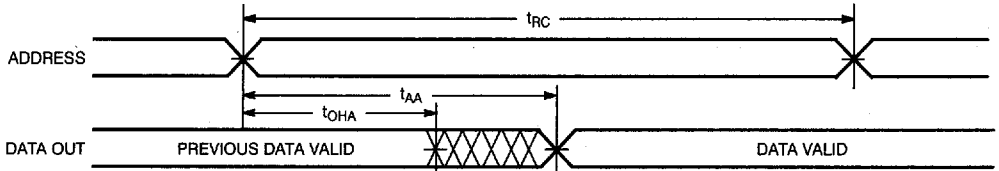
Switching Characteristics Over the Operating Range<sup>[4, 7, 8]</sup>

Parameter	Description	7C161A-15 7C162A-15		7C161A-20 7C162A-20		7C161A-25 7C162A-25		7C161A-35 7C162A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		15		20		25		35	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		5		5		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		7		10		12		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z	0		3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to HIGH Z		8		8		10		12	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	3		5		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		8		8		10		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
<b>WRITE CYCLE<sup>[11]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	15		20		20		25		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		10		10		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup> (7C162A)	3		5		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[9, 10]</sup> (7C162A)		7		7		7		10	ns
t <sub>DWE</sub>	$\overline{WE}$ LOW to Data Valid (7C161A)		15		20		25		30	ns
t <sub>ADV</sub>	Data Valid to Output Valid (7C161A)		15		20		20		30	ns
t <sub>DCE</sub>	$\overline{CE}$ LOW to Data Valid (7C161A)		15		20		25		35	ns

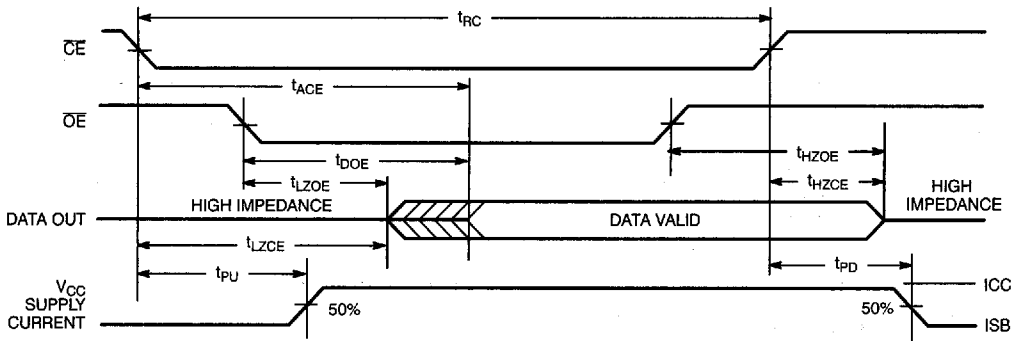
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Notes:

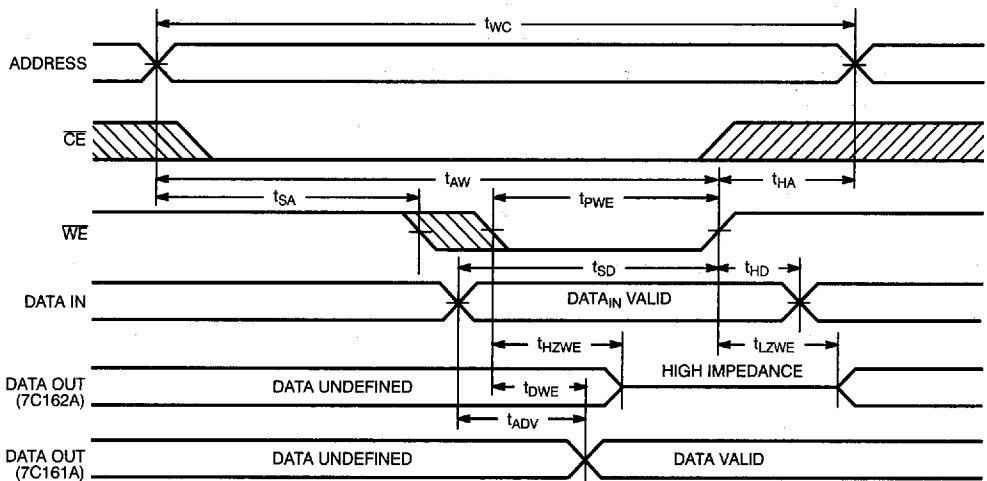
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- Both  $\overline{CE}_1$  and  $\overline{CE}_2$  are represented by  $\overline{CE}$  in the Switching Characteristics and Waveforms sections.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  LOW, and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms<sup>[8]</sup>**
**Read Cycle No. 1<sup>[12, 13]</sup>**


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**Read Cycle No. 2<sup>[12, 14]</sup>**


C161A-7

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[11]</sup>**


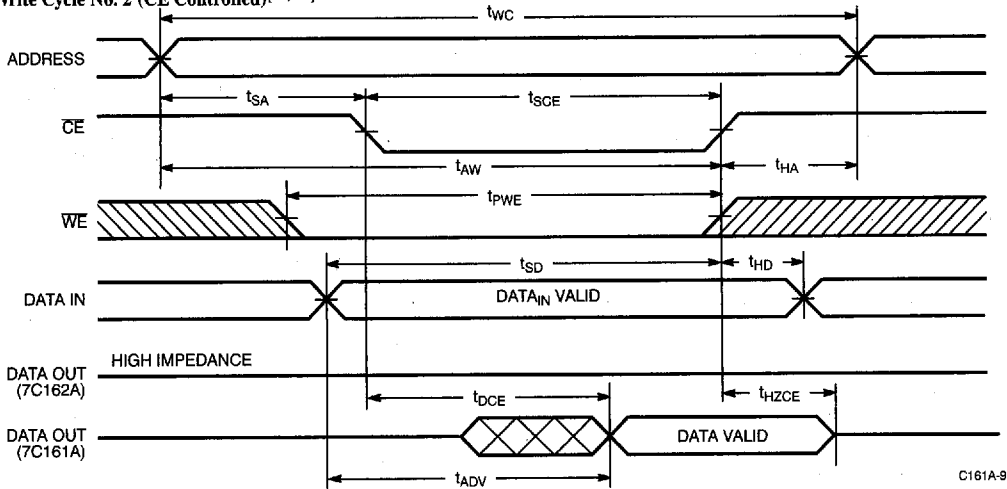
C161A-8

**Notes:**

 12.  $\overline{WE}$  is HIGH for read cycle.

 13. Device is continuously selected,  $\overline{CE}_1, \overline{CE}_2 = V_{IL}$ .

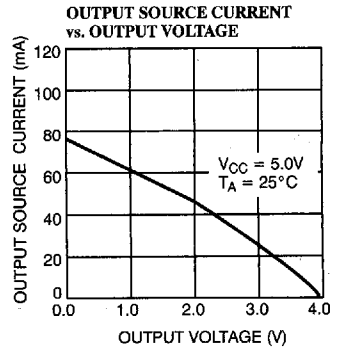
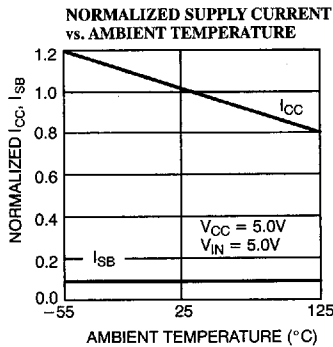
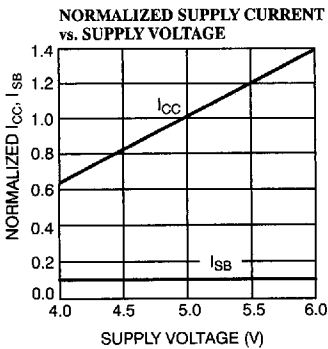
 14. Address valid prior to or coincident with  $\overline{CE}_1, \overline{CE}_2$  transition LOW.

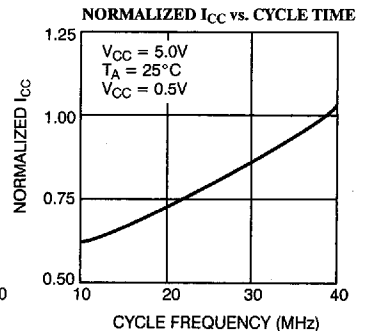
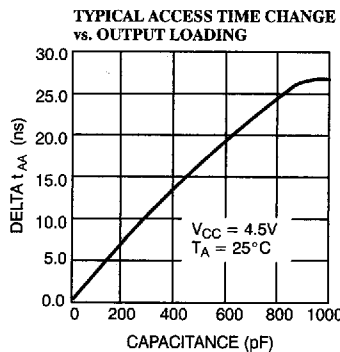
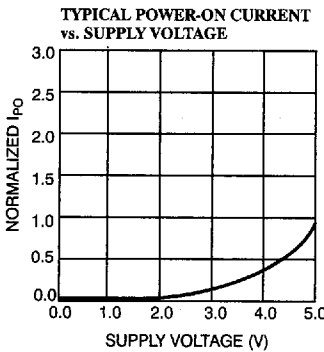
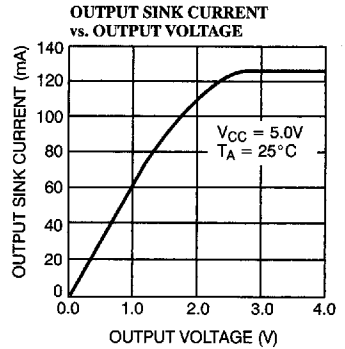
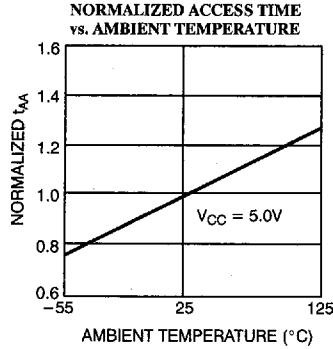
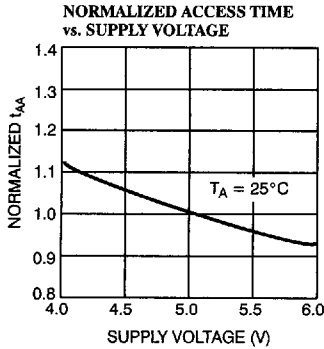
**Switching Waveforms (continued)**
**Write Cycle No. 2 (CE Controlled)<sup>[11, 15]</sup>**


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**Note:**

15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state (7C162A only).

**Typical DC and AC Characteristics**


**Typical DC and AC Characteristics (continued)**

**Address Designators**

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C161A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C161A-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C161A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
35	CY7C161A-35DMB	D22	28-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C162A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C162A-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C162A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C162A-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C162A-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded areas contain preliminary information.

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL Max.</sub>	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>OS</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OHA</sub>	7, 8, 9, 10, 11
t <sub>ACE</sub>	7, 8, 9, 10, 11
t <sub>DOE</sub>	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11
t <sub>DWE</sub> <sup>[16]</sup>	7, 8, 9, 10, 11
t <sub>ADV</sub>	7, 8, 9, 10, 11

Notes:

16. 7C161A only.