# 4M (512K x 8) Static RAM

## Features

- **Wide voltage range: 2.7V–3.6V**
- **Ultra low active power**
- **Low standby power**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a 32 pin TSOPII and a 32-pin SOIC package**

## Functional Description[1]

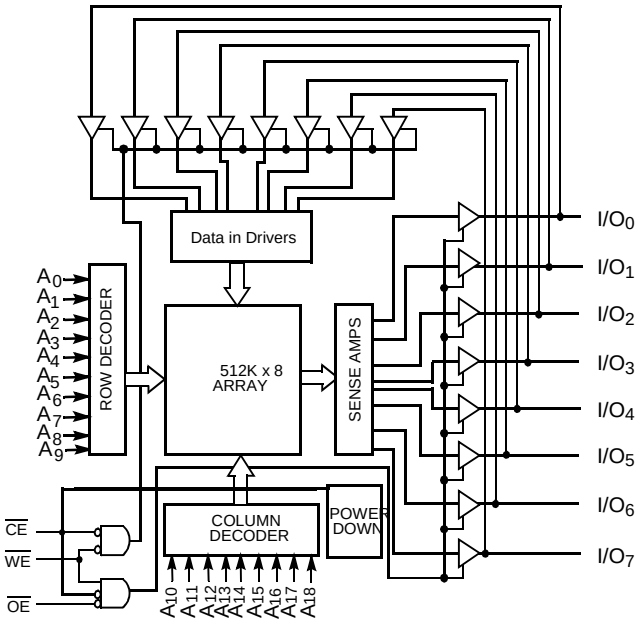
The CY62148V is a high-performance CMOS static RAM organized as 512K words by eight bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins ($I/O_0$ through $I/O_7$) is then written into the location specified on the address pins ($A_0$ through $A_{18}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ($I/O_0$ through $I/O_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

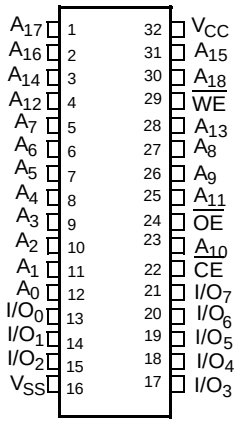
## Logic Block Diagram




**Note:**
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

## Pin Configurations

TSOPII/SOIC
Top View




## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2] .....–0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[2] .....–0.5V to $V_{CC}$ + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40°C to +85°C | 2.7V to 3.6V |

## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$, (mA) | | Standby $I_{SB2}$, (µA) | |
| | Min. | Typ.[3] | Max. | | Typ.[3] | Maximum | Typ.[3] | Maximum |
| CY62148VLL | 2.7 | 3.0 | 3.6 | 70 | 7 | 15 | 2 | 20 |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | CY62148V-70 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[3] | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.7V | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.7V | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | $V_{CC}$ = 3.6V | 2.2 | | $V_{CC}$ + 0.5V | V |
| $V_{IL}$ | Input LOW Voltage | | $V_{CC}$ = 2.7V | –0.5 | | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | ±1 | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | –1 | +1 | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ CMOS Levels | $V_{CC}$ = 3.6V | | 7 | 15 | mA |
| | | $I_{OUT}$ = 0 mA, f = 1 MHz CMOS Levels | | | 1 | 2 | mA |
| $I_{SB1}$ | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f = $f_{MAX}$ | | | 2 | 20 | µA |
| $I_{SB2}$ | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.3V<br>$V_{IN}$ ≥ $V_{CC}$ – 0.3V<br>or $V_{IN}$ ≤ 0.3V, f = 0 | $V_{CC}$ = 3.6V | | | | |

**Notes:**

2. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ.)}$, $T_A$ = 25°C.

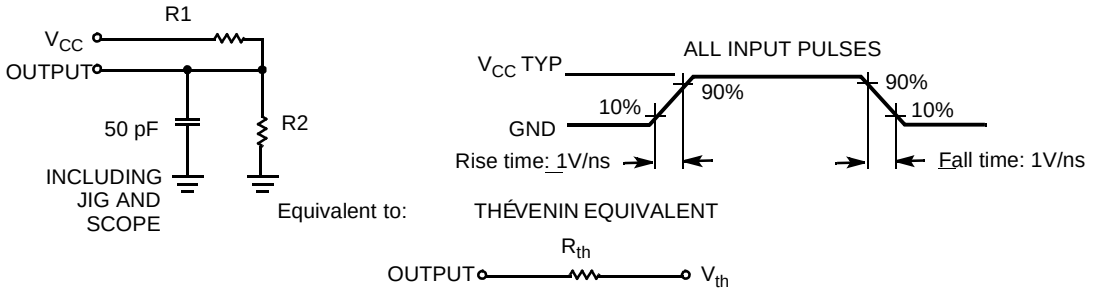
## Capacitance[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.0V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

## Thermal Resistance

| Parameter | Description | Test Conditions | Others | BGA | Units |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance[4] (Junction to Ambient) | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | TBD | TBD | °C/W |
| $\Theta_{JC}$ | Thermal Resistance[4] (Junction to Case) | | TBD | TBD | °C/W |

## AC Test Loads and Waveforms

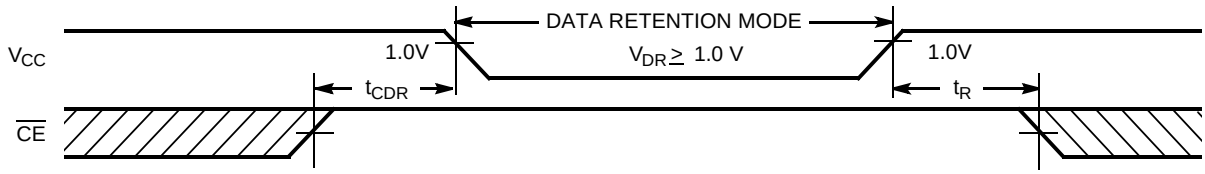



| Parameters | 3.0V | Unit |
|---|---|---|
| R1 | 1105 | Ohms |
| R2 | 1550 | Ohms |
| $R_{TH}$ | 645 | Ohms |
| $V_{TH}$ | 1.75V | Volts |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min. | Typ.[3] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 1.0 | | 3.6 | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 1.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$; No input may exceed $V_{CC}$ + 0.3V | | 0.2 | 5.5 | µA |
| $t_{CDR}$[4] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$[5] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform



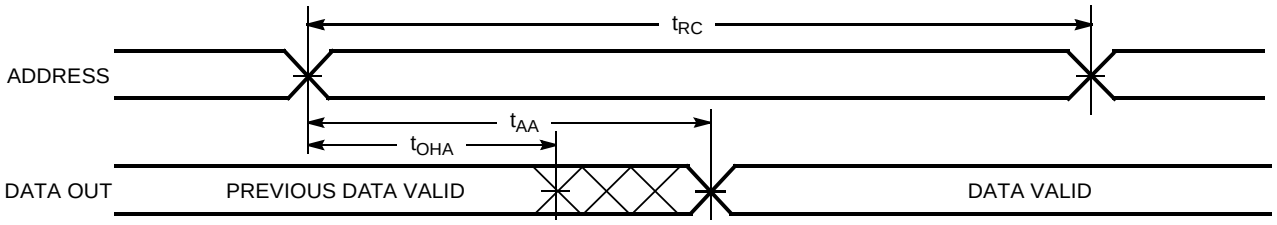

**Notes:**
4. Tested initially and after any design or process changes that may affect these parameters.
5. Full-device AC operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 10$ µs or stable at $V_{CC(min.)} \geq 10$ µs.

## Switching Characteristics Over the Operating Range [6]

| Parameter | Description | CY62148V-70 | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low-Z[7] | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High-Z[8] | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low-Z[7] | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High-Z[7, 8] | | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-down | | 70 | ns |
| **Write Cycle**[9, 10] | | | | |
| $t_{WC}$ | Write Cycle Time | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 60 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 50 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[7, 8] | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[7] | 10 | | ns |

## Switching Waveforms

**Read Cycle No. 1** [11, 12]

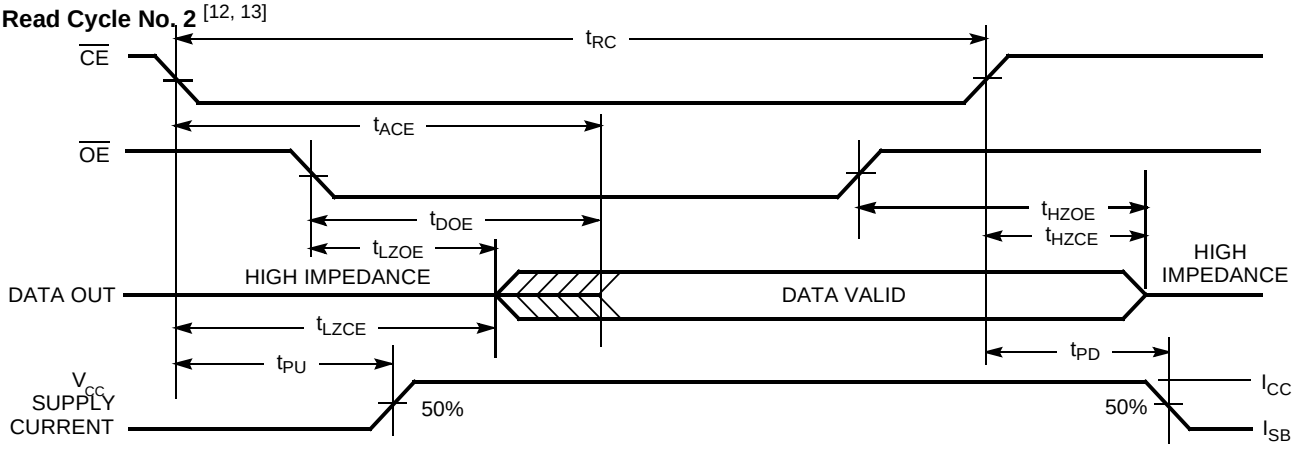



**Notes:**

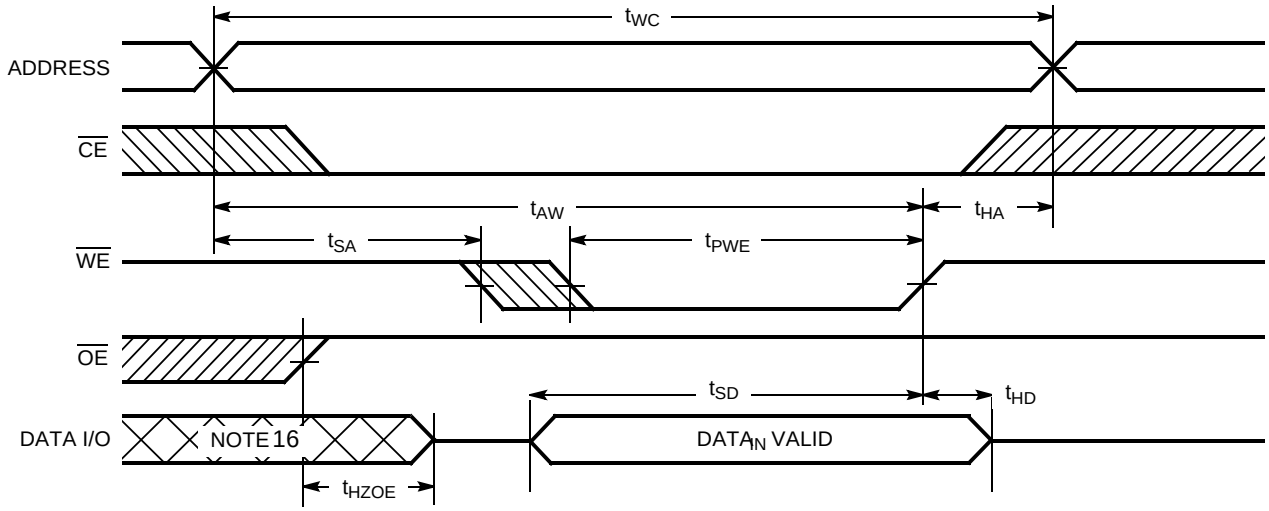
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance.
7. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
8. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms (continued)

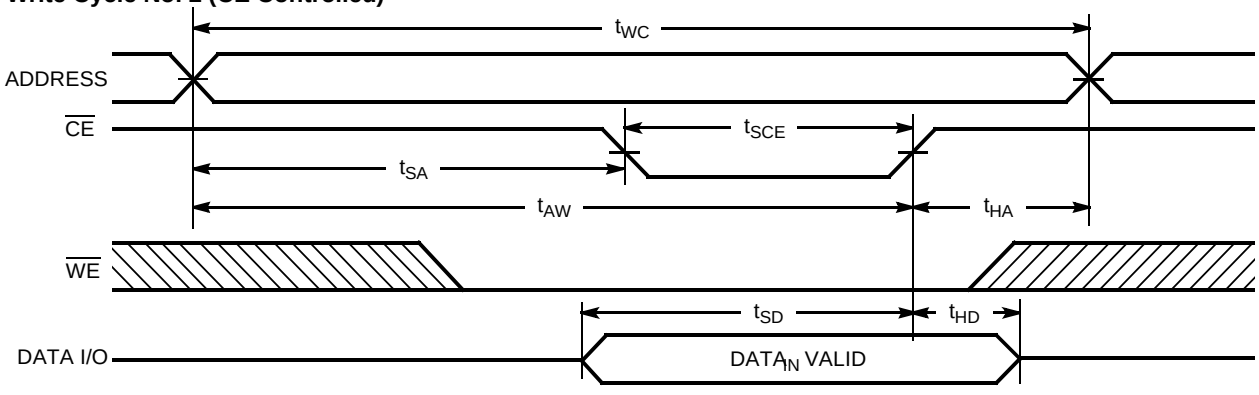
### Read Cycle No. 2 [12, 13]




### Write Cycle No. 1 (WE Controlled) [9, 14, 15]




### Write Cycle No. 2 (CE Controlled) [9, 14, 15]

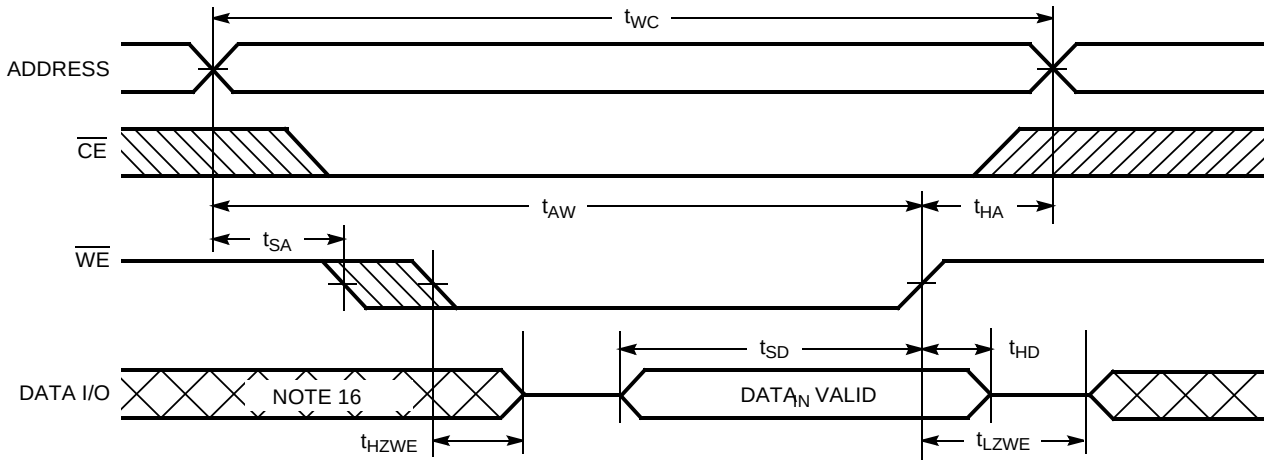



**Notes:**

11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

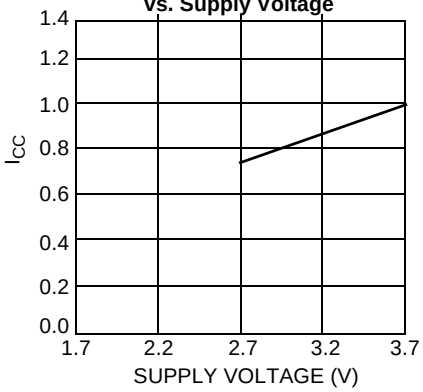
## Switching Waveforms (continued)

**Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [10, 15]

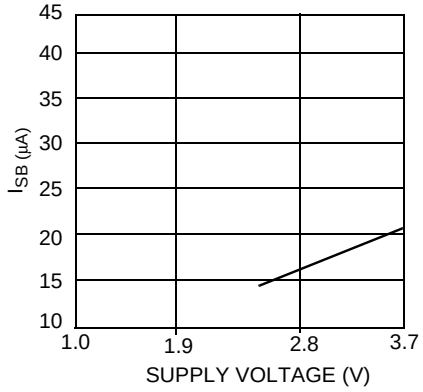



## Typical DC and AC Characteristics

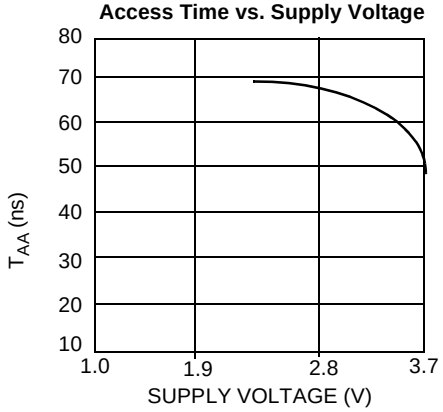
**Normalized Operating Current vs. Supply Voltage**




**Standby Current vs. Supply Voltage**




**Access Time vs. Supply Voltage**



## Truth Table

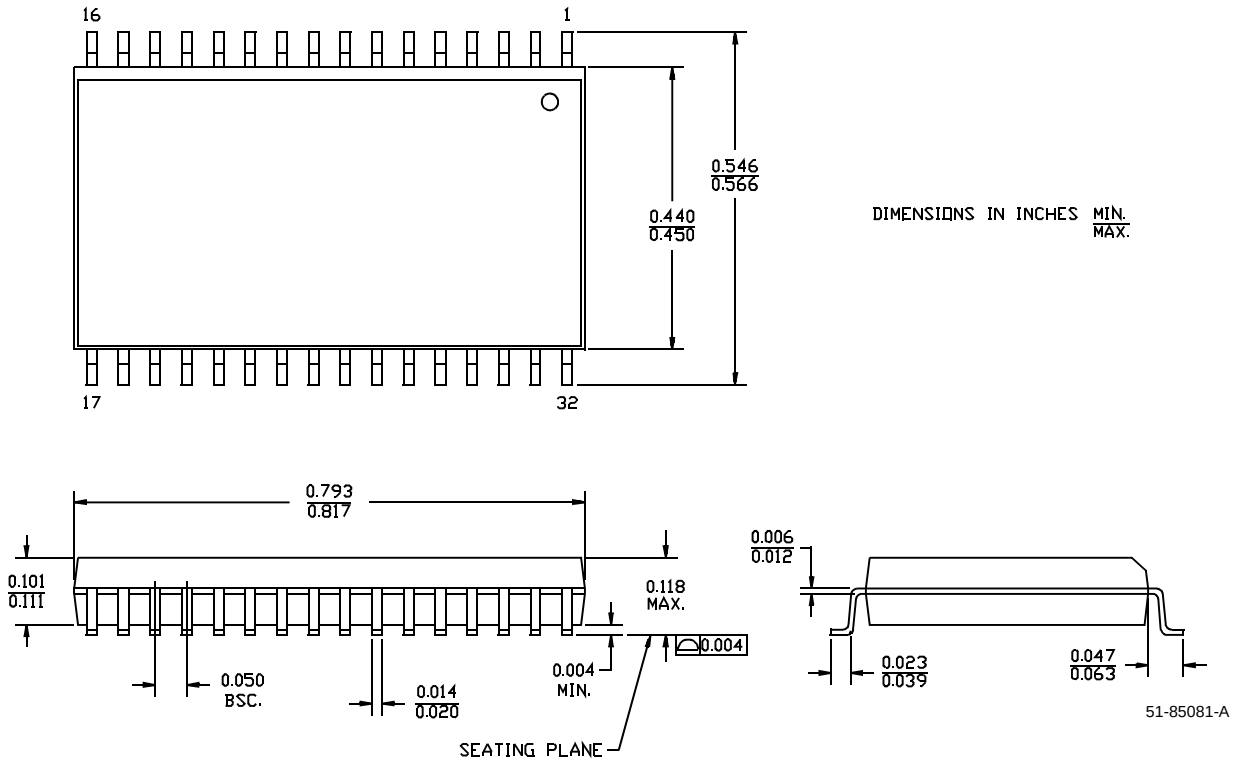
| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | L | X | Data In | Write | Active ($I_{CC}$) |
| L | H | H | High-Z | Output Disabled | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 70 | CY62148VLL-70ZI | ZS32 | 32-lead TSOPII | Industrial |
| | CY62148VLL-70SI | S34 | 32-lead 450-mil. molded SOIC | |

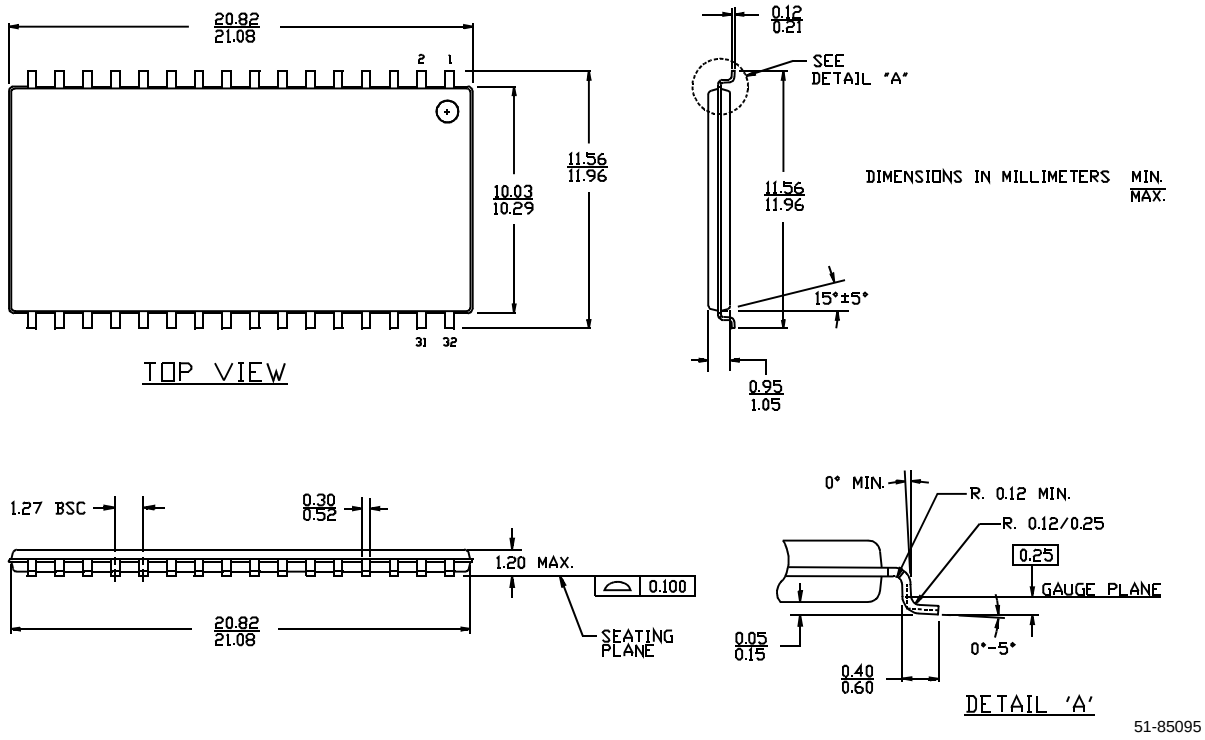
## Package Diagrams

**32-Lead (450-mil) Molded SOIC S34**



## Package Diagrams (continued)

**32-lead TSOP II ZS32**

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| Document Title: CY62148V MoBL® 4M (512K x 8) Static RAM<br>Document Number: 38-05070 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 107263 | 09/15/01 | SZV | Changed from Spec number: 38-00646 to 38-05070 |
| *A | 116515 | 09/04/02 | GBI | Added footnote 1.<br>Deleted fBGA package.<br>Removed fBGA package (replacement fBGA package is available in CY62148CV30) |