REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, part of 5 year review. ksr	06-10-26	Raymond Monnin
B	Update drawing to meet current MIL-PRF-38535 requirements. – glg	15-06-10	Charles Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
89-10-16

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 STATIC RAM (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89690**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89690	01	J	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Acess time
01	1/	2K X 8 CMOS SRAM	25 ns
02	1/	2K X 8 CMOS SRAM	20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	dual-in-line package
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
X	CQCC1-N32	32	rectangular chip carrier package
Y	See Figure 1	24	rectangular chip carrier package
Z	CQCC3-N28	28	rectangular chip carrier package
3	CQCC1-N28	28	rectangular chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC})	-0.5 V dc to 7 V dc
Input voltage range 2/	0.5 V to V_{CC} +0.5 V
Output voltage range in high impedance state	-0.5 V dc to 7 V dc
Output current	20 mA
Storage temperature range	-65°C to +150°C
Power dissipation, (P_D)	864 mW
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (Θ_{JC}):.	
Cases J, K, L, X, Z, and 3	See MIL-STD-1835
Case Y	20°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level Input voltage range (V_{IH})	2.2 V dc minimum to V_{CC} + 0.5 V dc maximum
Low level Input voltage range (V_{IL}) 3/	-0.5 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

2/ All voltages are with respect to GND.

3/ V_{IL} (minimum) of -3 V dc for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below -1 V dc will result in excessive currents that may damage the device.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.4 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$, $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), $V_{CC} = 5.5\ V$, $\overline{CE} = V_{IL}$, All other inputs at V_{IL}	1, 2, 3	01		135	mA
				02		150	
Standby power supply current TTL	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, $V_{CC} = 5.5\ V$, f = 0 MHz	1, 2, 3	01		45	mA
				02		50	
Standby power supply current CMOS	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, f = 0 MHz, $V_{CC} = 5.5\ V$, all other inputs $< 0.2\ V$ or $> (V_{CC} - 0.2\ V)$	1, 2, 3	All		20	mA
Input leakage current, any input	I_{ILK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1, 2, 3	All	-10	10	µA
Off-state output leakage current	I_{OLK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1, 2, 3	All	-10	10	µA
Output high voltage	V_{OH}	$I_{OUT} = -4.0\ mA$, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	$I_{OUT} = 8.0\ mA$, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1, 2, 3	All		0.4	V
Input capacitance 5/	C_{IN}	$V_{IN} = 0\ V$, f = 1.0 MHz, $T_C = 25°C$, See 4.3.1c	4	All		8.0	pF
Output capacitance 5/	C_{OUT}	$V_{OUT} = 0\ V$, f = 1.0 MHz, $T_C = 25°C$, See 4.3.1c	4	All		8.0	pF
Read cycle time	t_{AVAV}		9, 10, 11	01	25		ns
				02	20		
Address access time	t_{AVQV}		9, 10, 11	01		25	ns
				02		20	
Output hold after address change	t_{AVQX}		9, 10, 11	01	0		ns
				02	0		
Output enable to output active 5/ 6/	t_{OLQX}		9, 10, 11	01	0		ns
				02	0		
Output enable access time	t_{OLQV}		9, 10, 11	01		16	ns
				02		15	
Chip enable to output active 5/ 6/	t_{ELQX}		9, 10, 11	01	0		ns
				02	0		
Chip enable access time	t_{ELQV}		9, 10, 11	01		25	ns
				02		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$, $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to output in high - Z 5/ 6/	t_{EHQZ}		9, 10, 11	01		15	ns
				02		15	
Write recovery time	t_{WHAV}		9, 10, 11	01	0		ns
				02	0		
Chip enable to end-of-write	t_{ELWH}		9, 10, 11	01	20		ns
				02	15		
Address valid to end-of-write	t_{AVWH}		9, 10, 11	01	20		ns
				02	15		
Address to $\overline{WE}$ setup time	t_{AVWL}		9, 10, 11	01	0		ns
				02	0		
Address to $\overline{CE}$ setup time	t_{AVEL}		9, 10, 11	01	0		ns
				02	0		
Output enable to output In high - Z 5/ 6/	t_{OHQZ}		9, 10, 11	01		16	ns
				02		15	
Write enable pulse width	t_{WLWH}		9, 10, 11	01	20		ns
				02	15		
Data setup to end-of-write	t_{DVWH}		9, 10, 11	01	15		ns
				02	12		
Data hold after end-of-write	t_{WHDX}		9, 10, 11	01	0		ns
				02	0		
Chip enable pulse width during write	t_{ELEH}		9, 10, 11	01	20		ns
				02	15		
Write enable pulse setup time	t_{WLEH}		9, 10, 11	01	20		ns
				02	15		
Write to output in high-Z 5/ 6/	t_{WLQZ}		9, 10, 11	01		15	ns
				02		15	

1/ All voltages referenced to V_{SS}.

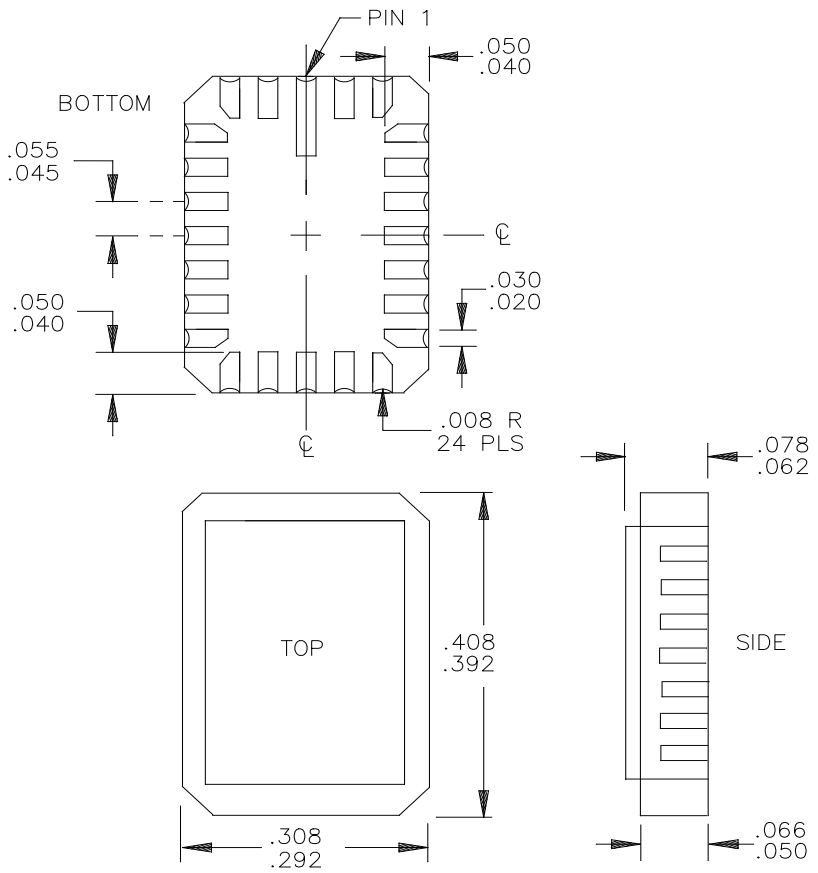
2/ Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 50 ns pulse width.

3/ AC measurements assume transition time $\le$ 5 ns and input level are from V_{SS} to 3.0 V. Output load is specified on figure 4. Reference timing levels are 1.5 V.

4/ For timing waveforms, see figure 4.

5/ Tested initially and after any design and or process changes which may affect this parameters, and therefore shall be guaranteed to the limits specified in table I. Transition measured ±500 mV from steady-state value.

6/ This parameter measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF, see figure 4.



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

Inches	mm
.008	0.20
.020	0.50
.030	0.76
.040	1.01
.045	1.14
.050	1.27
.055	1.39
.062	1.57
.066	1.68
.078	1.98
.292	7.41
.308	7.82
.392	9.95
.408	10.36

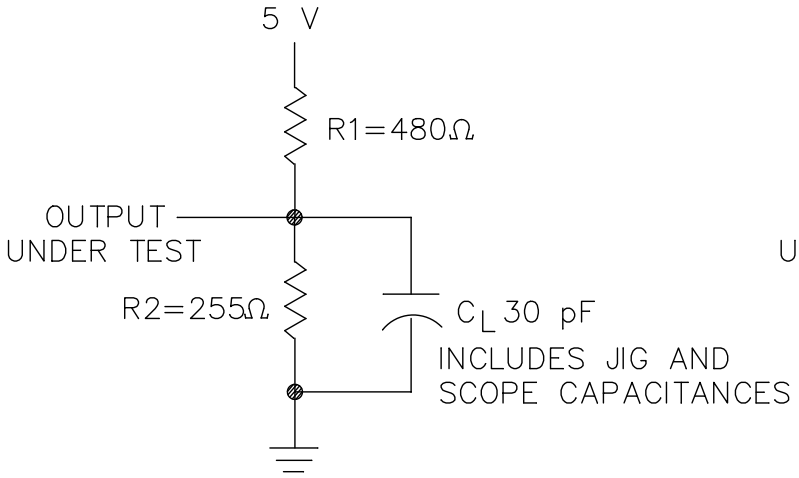
FIGURE 1. Case outline Y (24-terminal, .308" x .408" x .078"), rectangular chip carrier package.

Device types	01and 02		
Case outlines	J,K,L,Y	3, Z	X
Terminal number	Terminal Symbol		
1	A7	A7	NC
2	A6	A6	NC
3	A5	A5	NC
4	A4	A4	A7
5	A3	A3	A6
6	A2	A2	A5
7	A1	NC	A4
8	A0	NC	A3
9	I/O 0	A1	A2
10	I/O 1	A0	A1
11	I/O 2	I/O 1	A0
12	V_{SS}	I/O 2	NC
13	I/O 3	I/O 3	I/O 0
14	I/O 4	V_{SS}	I/O 1
15	I/O 5	I/O 4	I/O 2
16	I/O 6	I/O 5	V_{SS}
17	I/O 7	I/O 6	NC
18	$\overline{CE}$	I/O 7	I/O 3
19	A10	I/O 8	I/O 4
20	$\overline{OE}$	$\overline{CE}$	I/O 5
21	$\overline{WE}$	NC	I/O 6
22	A9	NC	I/O 7
23	A8	A10	$\overline{CE}$
24	V_{CC}	$\overline{OE}$	A10
25	- - -	$\overline{WE}$	$\overline{OE}$
26	- - -	A9	$\overline{WE}$
27	- - -	A8	NC
28	- - -	V_{CC}	A9
29	- - -	- - -	A8
30	- - -	- - -	NC
31	- - -	- - -	NC
32	- - -	- - -	V_{CC}

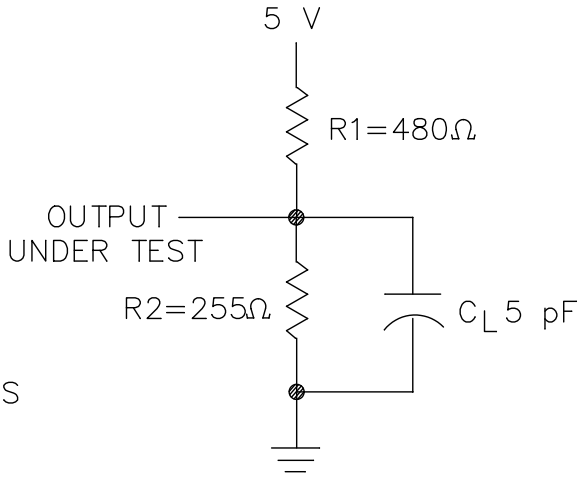
FIGURE 2. Terminal connections.

Inputs			I/O	Mode	Power
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O 0 - I/O 7		
H	X	X	HI - Z	Standby	Standby
L	H	L	Data output	Read	Active
L	H	H	HI - Z	Read	Active
L	L	X	Data input	Write	Active

FIGURE 3. Truth table.

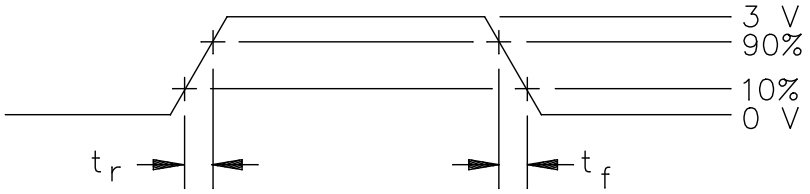


CONFIGURATION (a)
OR EQUIVALENT CIRCUIT



CONFIGURATION (b)
OR EQUIVALENT CIRCUIT

(FOR t_{ELQX}, t_{EHQZ}, t_{WLQZ}, t_{OLQX}, AND t_{OHQZ})

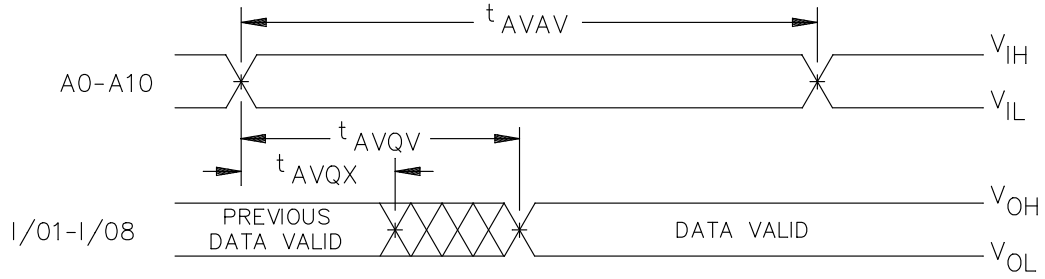


NOTES:

1. t_r and $t_f \leq 5$ ns.
2. All switching characteristics and timing requirements assume test conditions as depicted in configuration (a) and configuration (b) with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

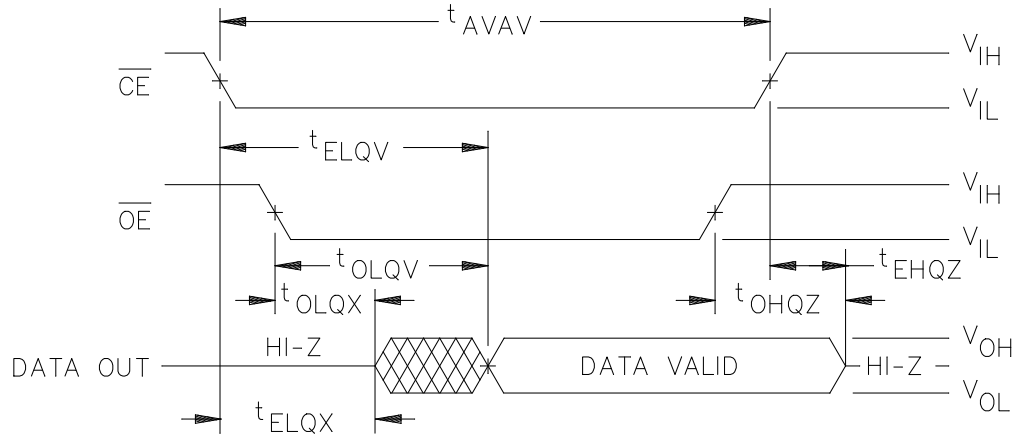
FIGURE 4. Load circuit and switching waveforms.

READ CYCLE TIMING FROM ADDRESS
SEE NOTE



NOTE: When $\overline{WE}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{CE}$.

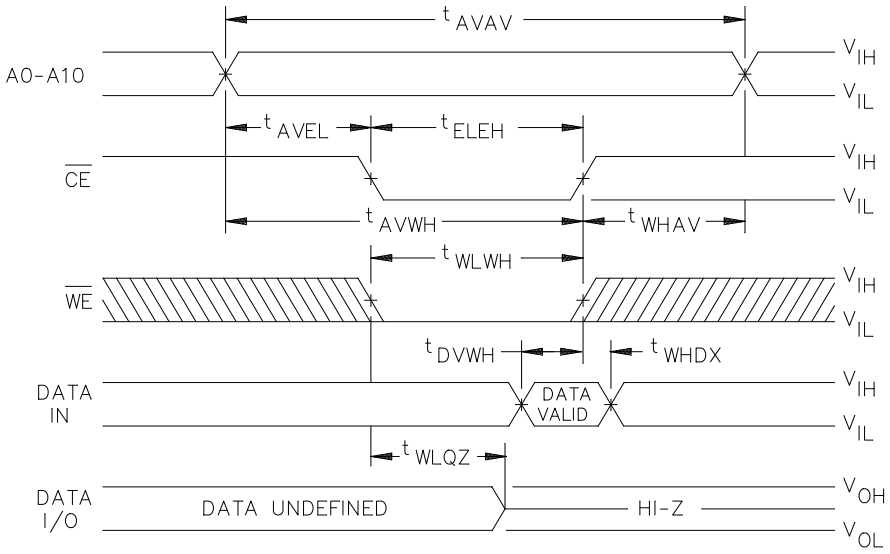
READ CYCLE TIMING FROM CHIP ENABLE
SEE NOTE



NOTE: When $\overline{WE}$ is high, address is valid prior to or simultaneously with the high to low transition of $\overline{CE}$.

FIGURE 4. Load circuit and switching waveforms - Continued.

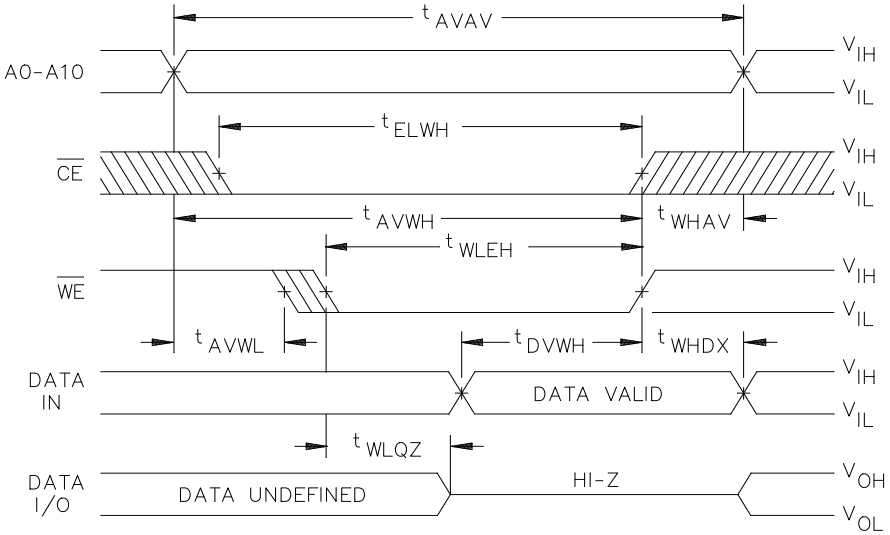
WRITE CYCLE TIMING CONTROLLED BY FROM CHIP ENABLE
SEE NOTE 1



NOTES: 1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

2. Data I/O pins enter high-impedance state, as shown when $\overline{CE}$ is held low during write.

WRITE CYCLE TIMING CONTROLLED BY WRITE ENABLE
SEE NOTE 1



NOTES: 1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

2. The internal write time of the memory if defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Data I/O pins enter high-impedance state, as shown when $\overline{CE}$ is held low during write.

FIGURE 4. Load circuit and switching waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10,11
Group A test requirements (method 5005)	1,2,3,4**,(7,8A,8B)***, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.

2/ ** see 4.3.1c.

3/ *** see 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-06-10

Approved sources of supply for SMD 5962-89690 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part number 2/
5962-8969001JA	3/ 3/ 3/	IDT6116SA25DB CY6116A-25DMB QP6116A-25DMB
5962-8969001KA	3/ 3/ 3/ 3DTT2	IDT6116SA25EB CY7C128A-25KMB QP7C128A-25KMB P4C116-25FMB
5962-8969001LA	3/ 3/ 61772 3DTT2 3/ 0C7V7	SMJ68CE16-25JDM CY7C128A-25DMB IDT6116SA25TDB P4C116-25DMB MT5C1608C-25883C QP7C128A-25DMB
5962-8969001XA	3/ 3/ 3/	CY6117A-25LMB IDT6116SA25L32B SMJ68CE16-25FGM
5962-8969001YA	3/ 3/ 3DTT2 3/	IDT6116SA25L24B CY7C128A-25LMB P4C116-25LMB QP7C128A-25LMB
5962-89690013A	3/ 3/ 3/ 3DTT2	CY6116A-25LMB IDT6116SA25L28B QP6116A-25LMB P4C116-25L28MB
5962-8969001ZA	3/	MT5C1608EC-25883C
5962-8969002JA	3/ 3/ 3/	IDT6116SA20DB CY6116A-20DMB QP6116A-20DMB
5962-8969002KA	3/ 3/ 3/ 3DTT2	IDT6116SA20EB CY7C128A-20KMB QP7C128A-20KMB P4C116-20FMB
5962-8969002LA	3/ 61772 3DTT2 3/ 0C7V7	CY7C128A-20DMB IDT6116SA20TDB P4C116-20DMB MT5C1608C-20883C QP7C128A-20DMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part number 2/
5962-8969002XA	3/ 3/	CY6117A-20LMB IDT6116SA20L32B
5962-8969002YA	3/ 3/ 3DTT2 3/	IDT6116SA20L24B CY7C128A-20LMB P4C116-20LMB QP7C128A-20LMB
5962-8969002ZA	3/	MT5C1608EC-20883C
5962-89690023A	3/ 3/ 3/ 3/ 3DTT2	CY6116A-20LMB IDT6116SA20L28B MT5C1608EC-20883C QP6116A-20LMB P4C116-20L28MB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	e2v, Inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035
3DTT2	Pyramid Semiconductor Corporation 1249 Reamwood Avenue Sunnyvale, CA 94089
61772	Integrated Device Technology, Inc. 6 Jenner STE 100 Irvine, CA 92618-3855