ICD2051

Dual Programmable Clock Oscillator

Single-Chip Programmable Oscillator Replaces Traditional Can Oscillators in Multi-Frequency or Variable Frequency Environments

- 2 Independent Clock Outputs Ranging from 320 KHz – 120 MHz
- Individually Programmable Oscillators Using a 22–bit Serial Word
- Low-Skew ÷1 and ÷2 Outputs, plus ÷4 CLKA Output
- Phase-Locked Loop Oscillator Input Derived from External Low-Frequency Reference Clock (1 MHz – 60 MHz) or External Crystal (2 MHz – 24 MHz)
- 3-State Oscillator Control Disables Outputs for Test Purposes (Optional)
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package Configurations

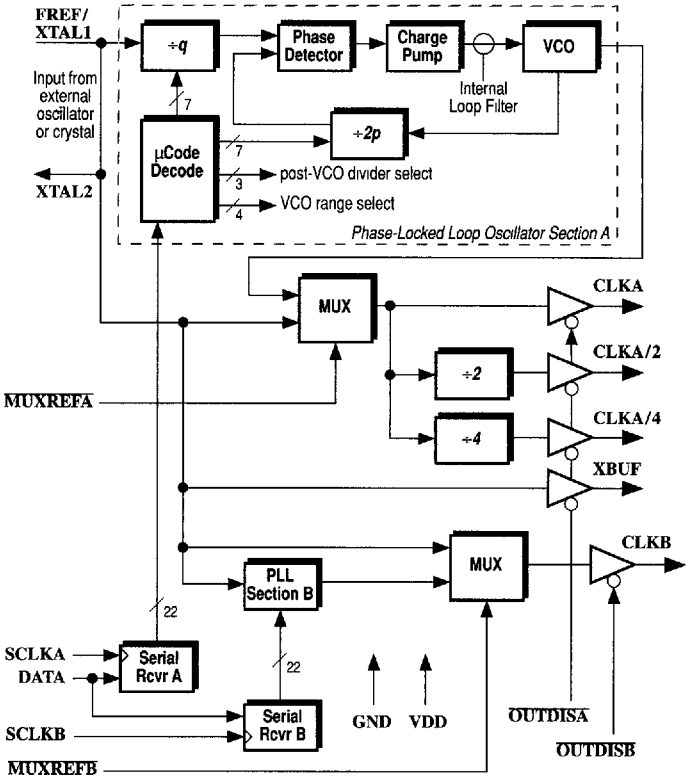

Fig. 1: ICD2051 Block Diagram

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Introduction

The ICD2051 Programmable Clock Generator offers 2 fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 320 KHz and 120 MHz. The ICD2051 is ideally suited for any design where one or more multiple or varying frequencies are required, replacing more expensive metal can oscillators.

The capability to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

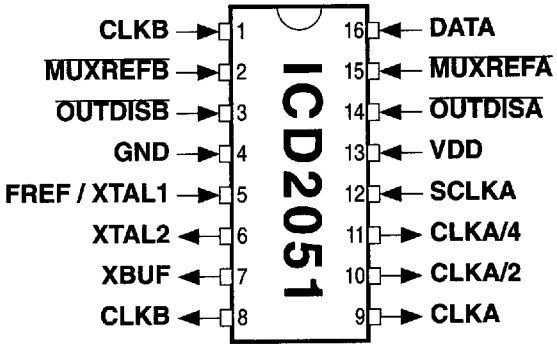

Table 1: Signal Descriptions

Pin #	Signal	Function
1	SCLKB	SCLKB is the serial clock input line for CLKB.
2	$\overline{\text{MUXREFB}}$	$\overline{\text{MUXREFB}}$ = 0, CLKB equals input reference frequency. $\overline{\text{MUXREFB}}$ = 1, CLKB equals programmed frequency. This is used if glitch-free frequency changes are required.
3	$\overline{\text{OUTDISB}}$	Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation is not required.)
4	GND	Ground
5	FREF / XTAL1	Input Reference Oscillator derived from available reference signal or attached crystal. (see XTAL2)
6	XTAL2	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator is used.)
7	XBUF	Buffered Crystal Oscillator Output. CMOS/TTL compatible.
8	CLKB	CLKB Programmable Oscillator Output
9	CLKA	CLKA Programmable Oscillator Output
10	CLKA/2	CLKA divided by 2. Note that this output has low skew with respect to the CLKA output.
11	CLKA/4	CLKA divided by 4.
12	SCLKA	SCLKA is the serial clock input line for CLKA.
13	VDD	+5V
14	$\overline{\text{OUTDISA}}$	Output Disable when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation is not required.)
15	$\overline{\text{MUXREFA}}$	$\overline{\text{MUXREFA}}$ = 0, CLKA equals input reference frequency. $\overline{\text{MUXREFA}}$ = 1, CLKA equals programmed frequency. This is used if glitch-free frequency changes are required.
16	DATA	Serial data input line for both programmable clock oscillators.

General Considerations

Programming the ICD2051

The desired output frequency is defined via a serial interface, with a 22-bit number shifted in. The ICD2051 has two programmable oscillators (CLKA and CLKB), requiring a 22-bit programming word (W) to be loaded into each channel independently. This word contains 5 fields:

Table 2: Programming Word Bit Fields

Field	# of Bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Reserved (R)	1	normally set to logic 1
Mux (M)	3	
Q Counter Value (Q')	7	LSB (Least Significant Bits)

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz)

The value of $f_{(VCO)}$ must remain between 40 MHz and 120 MHz inclusive. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Table 3: Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency.)

Table 4: Index Field (I)

I	f_{VCO} (MHz)
0000	40.0 – 42.5
0001	42.5 – 47.5
0010	47.5 – 53.5
0011	53.5 – 58.5
0100	58.5 – 62.5
0101	62.5 – 68.5
0110	68.5 – 69.0
0111	69.0 – 82.0
1000	82.0 – 87.0
1001	87.0 – 92.0
1010	92.0 – 92.1
1011	92.1 – 105.0
1100	105.0 – 115.0
1101	115.0 – 120.0
1110	115.0 – 120.0
1111	115.0 – 120.0

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

Programming Constraints

There are five primary programming constraints the user must be aware of:

$$1\text{MHz} \leq f_{(REF)} \leq 60\text{ MHz}$$

$$200\text{ KHz} \leq \frac{f_{(REF)}}{Q} \leq 1\text{ MHz}$$

$$40\text{ MHz} \leq f_{(VCO)} \leq 120\text{ MHz}$$

$$3 \leq Q \leq 129$$

$$4 \leq P \leq 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the ***BitCalc*** program, these constraints become transparent.

ICD2051 Programming Example

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The following is an example of the calculations ***BitCalc*** performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0111. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

Table 5: P & Q Value Candidates

P	Q	$f_{(VCO)}$ (MHz)	Error (ppm)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q) = (80,29) for best accuracy (40 ppm).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \quad (4dH)$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \quad (1bH)$$

and the full programming word, W, is:

$$W = I, P', R, M, Q' = 0111, 1001101, 1, 001, 0011011 = 01111001101100100011011 \quad (1e6c9bH)$$

A low-to-high transition on SCLKA/SCLKB (depending on appropriate channel) is used to shift the programming word W into DATA as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 22 shifts are performed, then only the last 22 data bits received will be retained.

Glitch-Free Frequency-Modification Procedure

When changing to a new frequency, there is a period of time when the output signal will be in transition and may glitch due to changes in the post divider. For applications where it is critical that the output clock not glitch and always maintain some known value, the $\overline{\text{MUXREFA}}$ and $\overline{\text{MUXREFB}}$ inputs must be used. Under normal operation, $\overline{\text{MUXREF(X)}}$ is high and the output clocks are at the programmed value. When $\overline{\text{MUXREF(X)}}$ is brought low, the reference clock is now multiplexed to the associated output clock. The output remains at this fixed frequency while the programmed frequency seeks its new value.

When programming the ICD2051, use the MUXREF inputs in the following manner:

1. Set $\overline{\text{MUXREF(X)}}$ to a low state. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See the timing specifications.)
2. Shift in the desired output frequency value via a 22-bit word (as defined above) using the appropriate SCLK and DATA lines.
3. After the last bit is shifted in, the VCO will settle to the new state (within .01% of the actual output frequency) within 10 msec.
4. Set $\overline{\text{MUXREF(X)}}$ to a high state. This will set the output to the new programmed frequency. The transition is guaranteed to be glitch-free. (See *Fig. 4: Serial Programming Timing* on page 257.)

Skew-Free ÷2 on CLKA

The CLKA output is available concurrently as ÷1, ÷2 and ÷4 values of the desired output. The ÷1 and ÷2 outputs are also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 2 ns of skew between the two outputs, with 1 ns or less available as an order option.

Output Frequency Accuracy

The accuracy of the ICD2051 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2051 are integrally related to the input reference frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2051 generally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (ppm) are given for any desired output frequency as part of the ***BitCalc*** program output.

3-State Output Operation

The $\overline{\text{OUTDISA}}$ or $\overline{\text{OUTDISB}}$ signal, when pulled low, will 3-state the clock output line (CLKA or CLKB respectively). This supports wired-or connections between external clock lines, and allows for procedures where the clock must be disabled, such as automated testing. The output disable signals contain internal pull-ups; they may be left unconnected if 3-state operation is not required.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2051.

Layout & Power Conditioning Considerations

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing any of the output traces of the ICD2051 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2051 closest to the device requiring the highest frequency.

A clean power supply is important, particularly at the higher frequencies. For best results, use either a +12V supply through a +5V Zener diode or a 3-pin +5V voltage regulator.

If a +12V supply is not available, then we recommend using a low-pass filter consisting of a capacitor and a 22Ω resistor. This method works quite well, but it has one drawback which must be allowed for, namely that there will be a frequency-dependent voltage drop across the resistor. The ICD2051 can operate over a very wide frequency range (300 KHz – 120 MHz), and operating power consumption depends on the frequency, ranging from a minimum of around 15 mA for very low frequencies on up to 100 mA at the top end. This results in a large frequency-dependent voltage drop across the RC circuit.

Thus, if the ICD2051 is to be used over a wide frequency range, use the voltage regulator method, running the device at the normal supply specification of +5V. If, on the other hand, the device is to be used over a narrow frequency range, and if the total power consumption is determined not to cause more than a 0.25V change across the RC filter (see the following section), then the filter method may be used.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I = C • V • f, where I=current, C=load capacitance (max. 25pF), V=output voltage (usually 5V), and f=output frequency (in MHz).

To calculate total operating current, sum the following:

XBUF ⇒ $C \cdot V \cdot f_{(REF)}$
CLKA ⇒ $C \cdot V \cdot f_{(CLKA)}$
CLKA/2 ⇒ $C \cdot V \cdot f_{(CLKA/2)}$
CLKA/4 ⇒ $C \cdot V \cdot f_{(CLKA/4)}$
CLKB ⇒ $C \cdot V \cdot f_{(CLKB)}$
Internal ⇒ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Typical values:

Table 6: Typical Load Current Values

Frequency	Load	Current (mA)
low	none	15
high	none	40
high	high	100

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All of the ICD2051 families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, both the synthesis blocks are physically separated into discrete elements, with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCOs are separated from the digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs (which tend to be the most demanding applications with regard to bit-jitter).

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2051 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2051, no manufacturing "tweaks" to external filter components are required as is the case with external filters.

Ordering Information

Table 7: Order Codes

Part Number	Package Type	Temperature Range
ICD2051	S = 16-Pin SOIC DIP	C = Commercial[a]

a. 0°C to +70°C

Example: order ICD2051SC for the ICD2051, 16-pin plastic SOIC, commercial temperature range device.

Device Specifications

Electrical Data

Table 8: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		525	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

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Table 9: DC Characteristics

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level CMOS output voltage	2.4		Volts	I_{OH} = –4.0 mA
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0 mA
I_{IH}	Input high current		150	µA	V_{IH} = 5.25V
I_{IL}	Input low current		–250	µA	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µA	(3-state)
I_{DD}	Power supply current	15	100	mA	
I_{DD-TYP}	Power supply current (typical)		50	mA	typ @ 50 MHz

Table 10: AC Characteristics

Symbol	Name	Description	Min	Max	Units
t_1	ref freq	Reference Oscillator nominal value	1	60	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as $t_2 \div t_1$	40%	60%	
t_3	rise time	Rise time for the output oscillators into a 25pF load		3	ns
t_4	fall time	Fall time for the output oscillators into a 25pF load		3	ns
t_5	CLKA/2/4 skew	Skew delay between the CLKA output and the CLKA/2 & CLKA/4 outputs		2	ns
t_6	set-up	Delay required after MUXREF goes low prior to starting the SCLK clock line	t_{freq1}		ns
t_7	cycle time	Minimum cycle time for the SCLK clock	$2 \div t_1$		ns
t_{7H}	high time	Minimum high time for the SCLK clock	$1 \div t_1$		ns
t_{7L}	low time	Minimum low time for the SCLK clock	$1 \div t_1$		ns
t_8	clk stable	Time required for CLKA or CLKB oscillator to become valid after last SCLK clock		10	msec
t_9	set-up	Time required for the data to be valid prior to the rising edge of SCLK	10		ns
t_{10}	hold	Time required for the data to remain valid after the rising edge of SCLK	5		ns
t_{11}	transition	Time for CLKA or CLKB to go high after assertion of MUXREF	0	t_{freq1}	ns
t_{12}	transition	Delay of CLKA or CLKB prior to valid $t_{(REF)}$ signal at output	$\frac{t_{(REF)}}{2}$	$3\frac{t_{(REF)}}{2}$	ns
t_{13}	transition	Time for CLKA or CLKB to go high after release of MUXREF	0	$t_{(REF)}$	ns
t_{14}	transition	Delay of CLKA or CLKB prior to valid t_{freq2} signal at output	$\frac{t_{freq2}}{2}$	$3\frac{t_{freq2}}{2}$	ns
t_{15}	3-state	Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion		12	ns
t_{16}	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high		12	ns

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 3: Rise and Fall Times

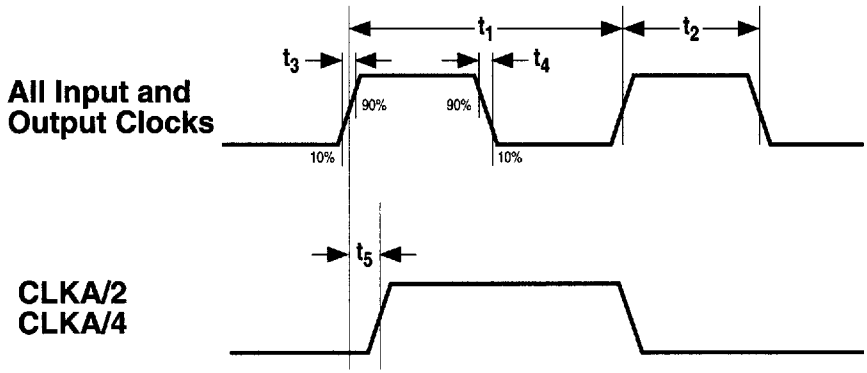

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Fig. 4: Serial Programming Timing

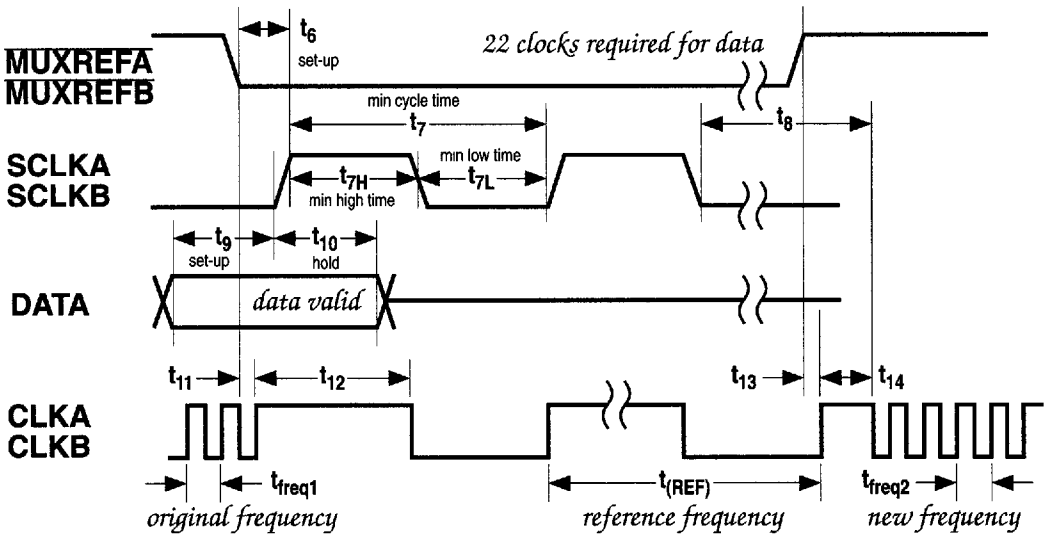
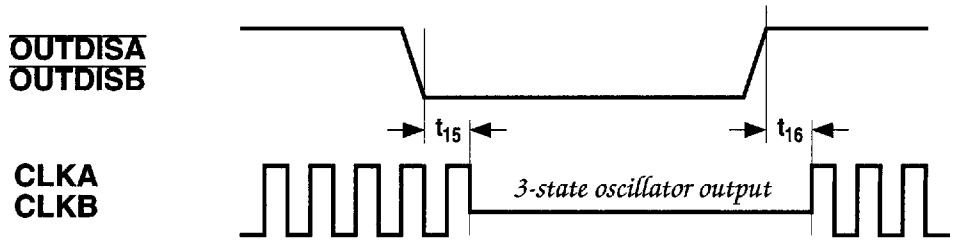


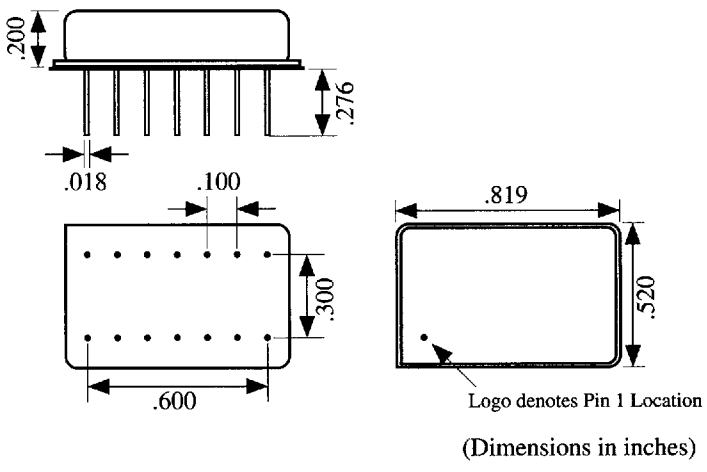
Fig. 5: 3-StateTiming



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

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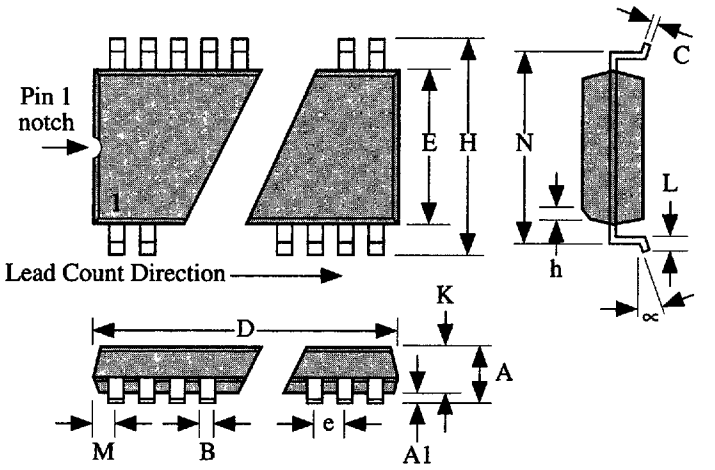
16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

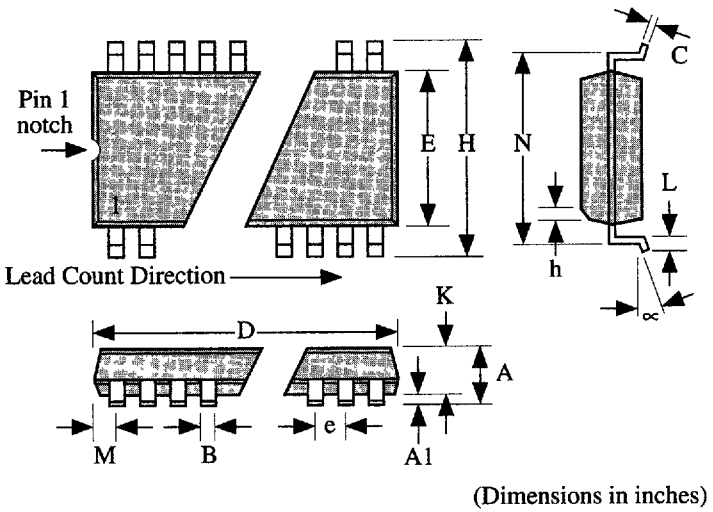


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x 45°	
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)

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