

## Features

- Temperature ranges:
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
  - Automotive-A: -40 °C to 85 °C
- High speed
  - 55 ns
- CMOS for optimum speed/power
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- Available in Pb-free 28-pin SNC package

## Functional Description

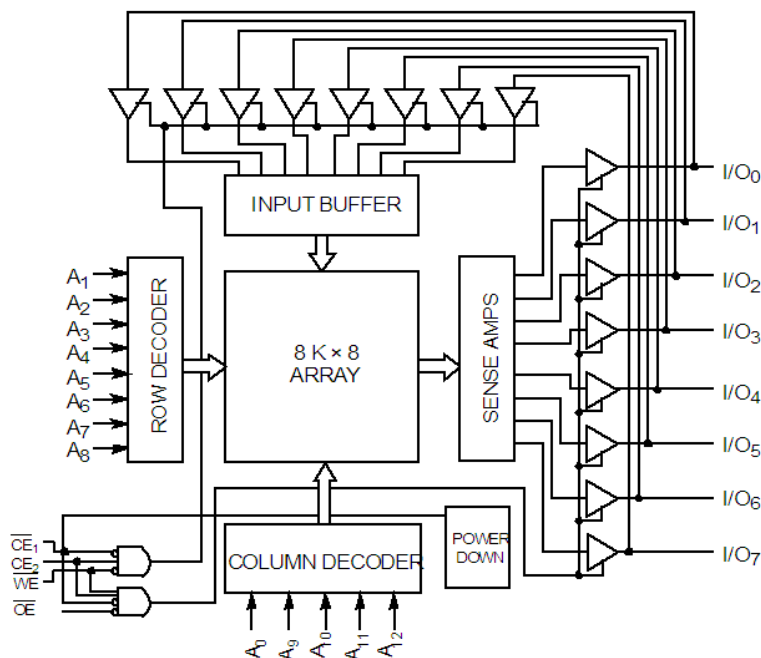
The CY6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. Both devices have an automatic power-down feature ( $\overline{CE}_1$ ), reducing the power consumption by over 70% when deselected. The CY6264 is packaged in a 450-mil (300-mil body) SOIC.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}_1$  and  $\overline{WE}$  inputs are both LOW and  $CE_2$  is HIGH, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{12}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}_1$  and  $\overline{OE}$  active LOW,  $CE_2$  active HIGH, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to ensure alpha immunity.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

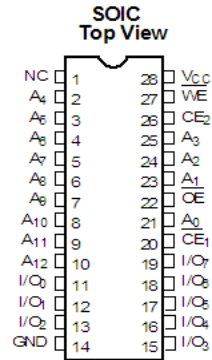


## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Package Diagram</b> .....	<b>13</b>
<b>Selection Guide</b> .....	<b>3</b>	<b>Acronyms</b> .....	<b>14</b>
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>14</b>
<b>Operating Range</b> .....	<b>4</b>	Units of Measure .....	14
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document History Page</b> .....	<b>15</b>
<b>Capacitance</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>16</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	Worldwide Sales and Design Support .....	16
<b>Switching Characteristics</b> .....	<b>6</b>	Products .....	16
<b>Switching Waveforms</b> .....	<b>7</b>	PSoC® Solutions .....	16
<b>Typical DC and AC Characteristics</b> .....	<b>10</b>	Cypress Developer Community .....	16
<b>Truth Table</b> .....	<b>11</b>	Technical Support .....	16
<b>Address Designators</b> .....	<b>11</b>		
<b>Ordering Information</b> .....	<b>12</b>		
Ordering Code Definitions .....	12		

## Pin Configuration

Figure 1. 28-pin SOIC pinout (Top View)



## Selection Guide

Description	Range	-55	-70	Unit
Maximum access time		55	70	ns
Maximum operating current	Commercial	100	100	mA
	Industrial	260	200	mA
	Automotive-A	–	200	mA
Maximum CMOS standby current	Commercial	15	15	mA
	Industrial	30	30	mA
	Automotive-A	–	30	mA

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied ..... -55 °C to +125 °C
- Supply voltage to ground potential <sup>[1]</sup> ..... -0.5 V to +7.0 V
- DC voltage applied to outputs in high Z state <sup>[1]</sup> ..... -0.5 V to +7.0 V
- DC input voltage <sup>[1]</sup> ..... -0.5 V to +7.0 V
- Output current into outputs (LOW) ..... 20 mA

- Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V
- Latch-up current ..... > 200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	
Automotive-A	-40 °C to +85 °C	

### Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-55		-70		Unit	
			Min	Max	Min	Max		
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	V	
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	-	0.4	V	
V <sub>IH</sub>	Input HIGH voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V	
V <sub>IL</sub>	Input LOW voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	µA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , output disabled	-5	+5	-5	+5	µA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA	Commercial	-	100	-	100	mA
			Industrial	-	260	-	200	
			Automotive-A	-		-	200	
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ power-down current	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , Min duty cycle = 100%	Commercial	-	20	-	20	mA
			Industrial	-	50	-	40	
			Automotive-A	-		-	40	
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ power-down current	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3 V$ , $V_{IN} \geq V_{CC} - 0.3 V$ or $V_{IN} \leq 0.3 V$	Commercial	-	15	-	15	mA
			Industrial	-	30	-	30	
			Automotive-A	-		-	30	

**Note**

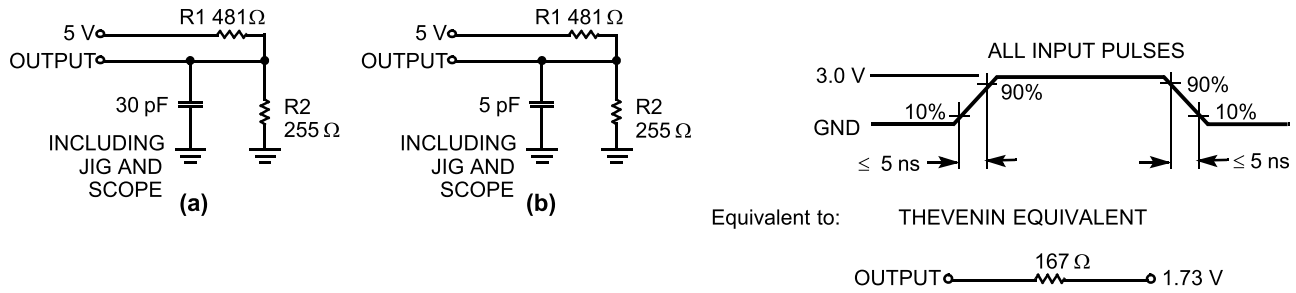
1. Minimum voltage is equal to -3.0 V for pulse durations less than 30 ns.

### Capacitance

Parameter [2]	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	7	pF
C <sub>OUT</sub>	Output capacitance		7	pF

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



**Note**

2. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[3]</sup>	Description	-55		-70		Unit
		Min	Max	Min	Max	
<b>READ CYCLE</b>						
$t_{RC}$	Read cycle time	55	–	70	–	ns
$t_{AA}$	Address to data valid	–	55	–	70	ns
$t_{OHA}$	Data hold from address change	5	–	5	–	ns
$t_{ACE1}$	$\overline{CE}_1$ LOW to data valid	–	55	–	70	ns
$t_{ACE2}$	$CE_2$ HIGH to data valid	–	40	–	70	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	–	35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z	3	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[4]</sup>	–	20	–	30	ns
$t_{LZCE1}$	$\overline{CE}_1$ LOW to low Z <sup>[5]</sup>	5	–	5	–	ns
$t_{LZCE2}$	$CE_2$ HIGH to low Z	3	–	5	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to high Z <sup>[4, 6]</sup> $CE_2$ LOW to high Z	–	20	–	30	ns
$t_{PU}$	$\overline{CE}_1$ LOW to power-up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH to power-down	–	25	–	30	ns
<b>WRITE CYCLE</b> <sup>[6, 7]</sup>						
$t_{WC}$	Write cycle time	50	–	70	–	ns
$t_{SCE1}$	$\overline{CE}_1$ LOW to write end	40	–	60	–	ns
$t_{SCE2}$	$CE_2$ HIGH to write end	30	–	50	–	ns
$t_{AW}$	Address setup to write end	40	–	55	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	25	–	40	–	ns
$t_{SD}$	Data setup to write end	25	–	35	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[4]</sup>	–	20	–	30	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z	5	–	5	–	ns

### Notes

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Switching Waveforms

Figure 3. Read Cycle No. 1 [8, 9]

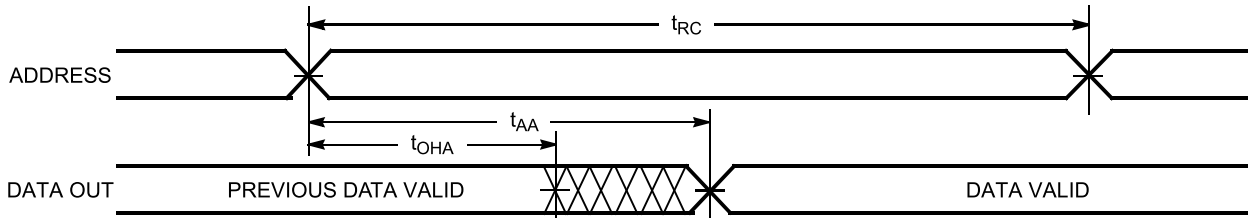
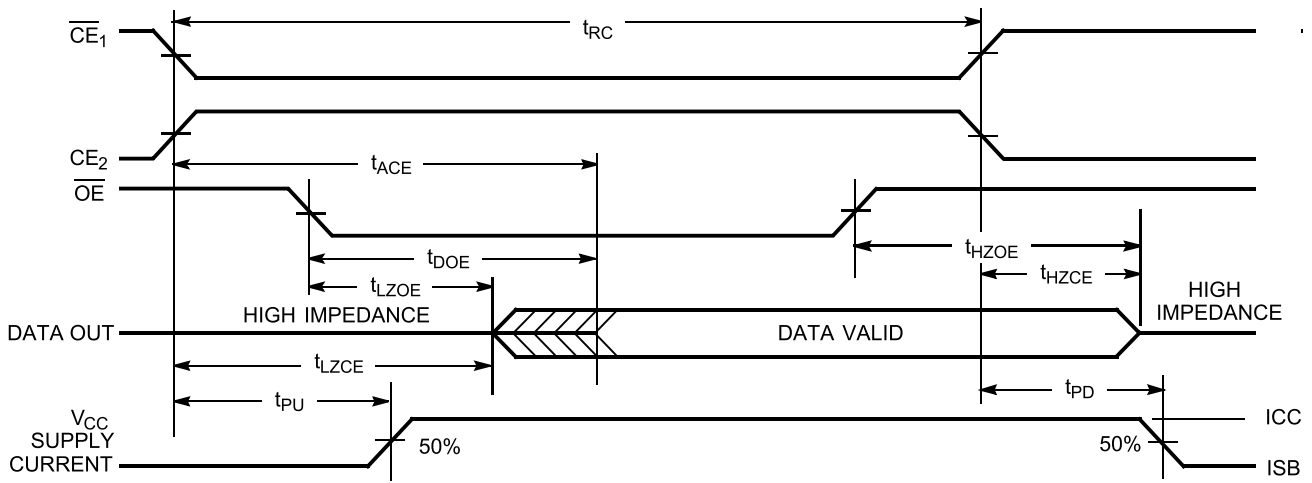


Figure 4. Read Cycle No. 2 [10, 11]



Notes

- 8. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .  $CE_2 = V_{IH}$ .
- 9. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 10.  $\overline{WE}$  is HIGH for read cycle.
- 11. Data I/O is High Z if  $\overline{OE} = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ , or  $\overline{WE} = V_{IL}$ .

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [12, 13]

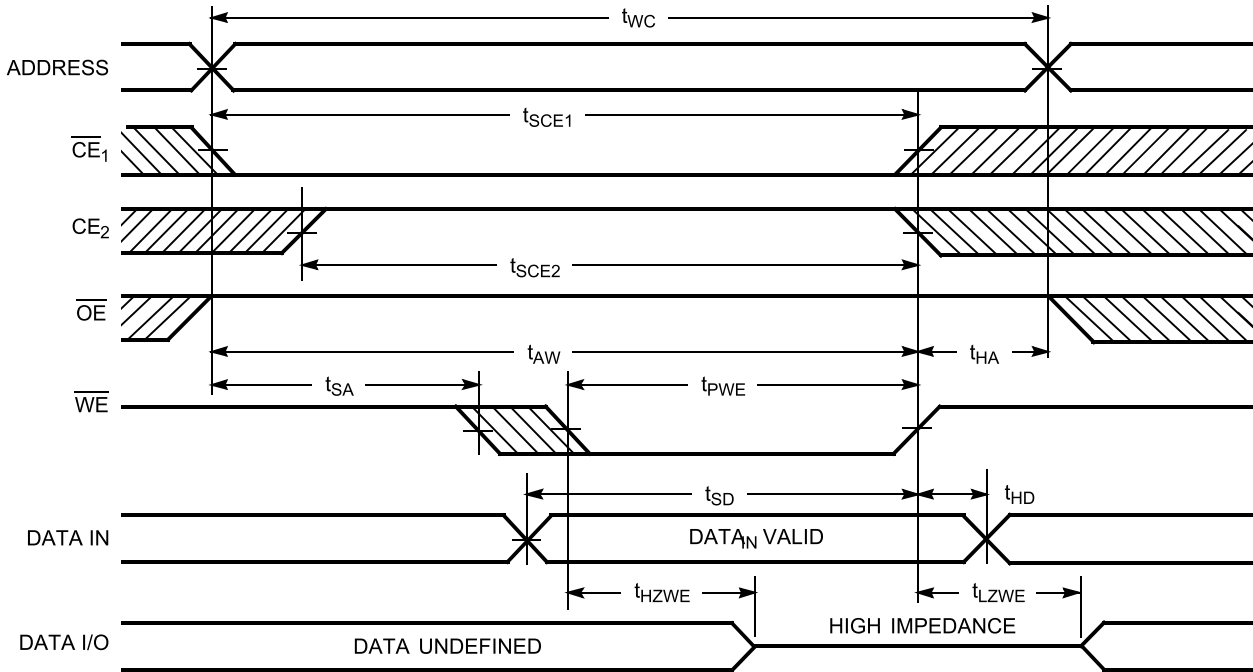
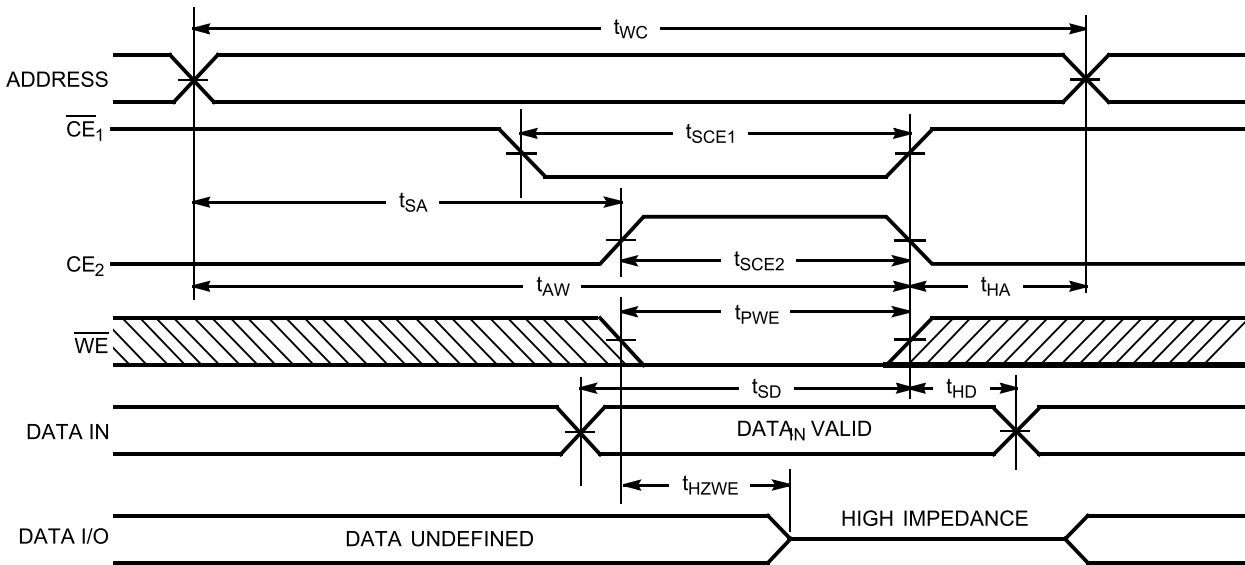


Figure 6. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [12, 13, 14]



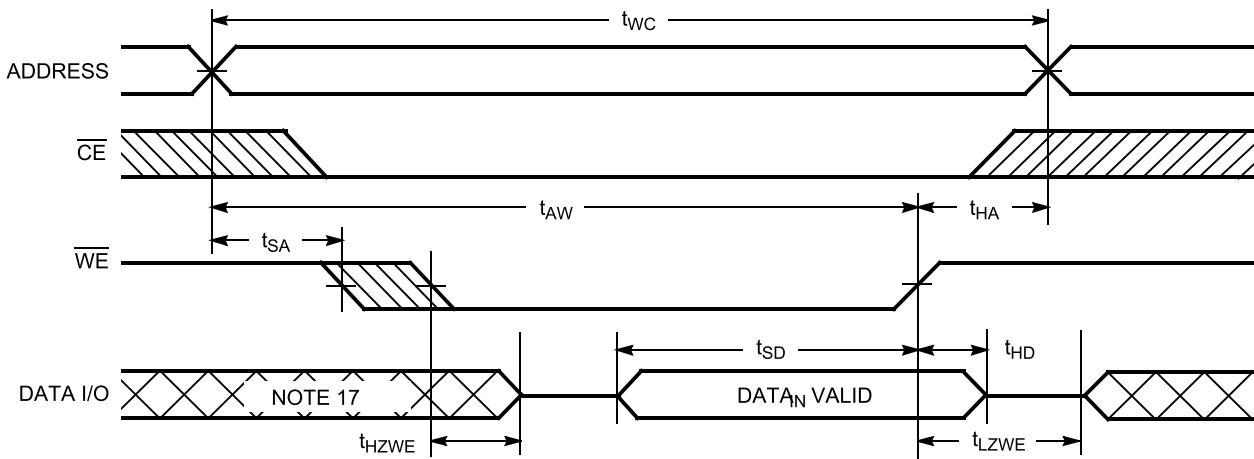
Notes

- 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 13. Data I/O is High Z if  $OE = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ , or  $WE = V_{IL}$ .
- 14. If  $\overline{CE}$  goes HIGH simultaneously with  $WE$  HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

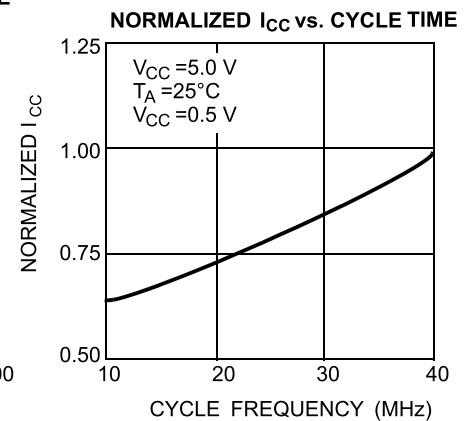
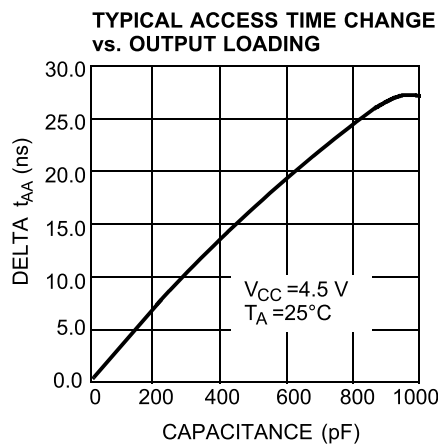
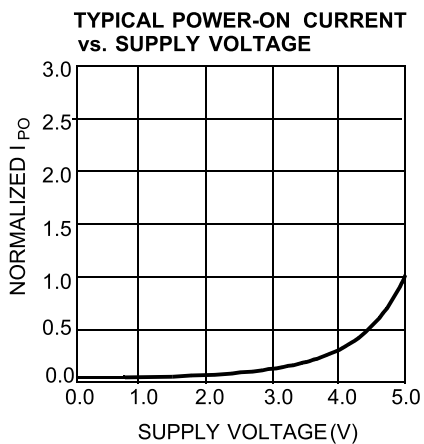
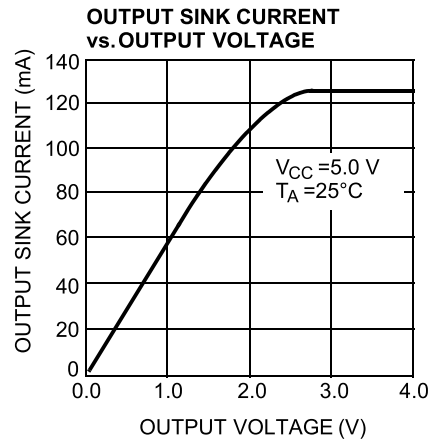
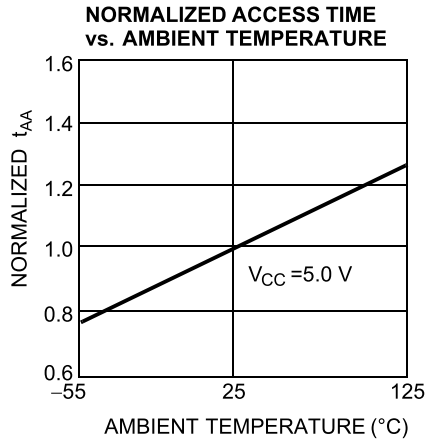
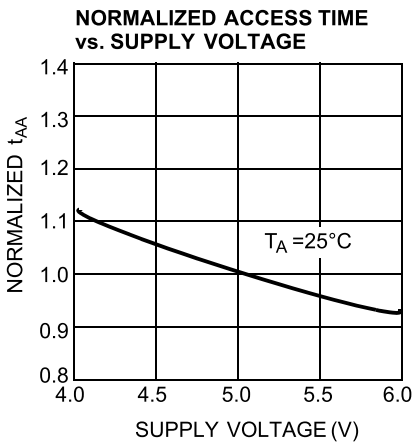
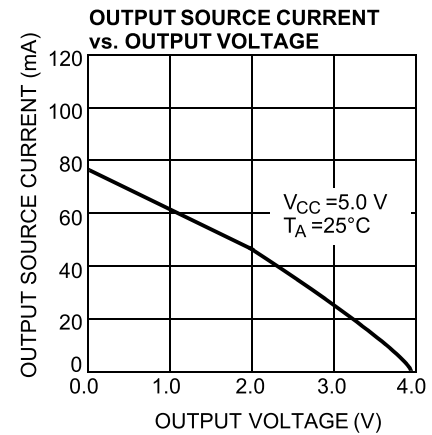
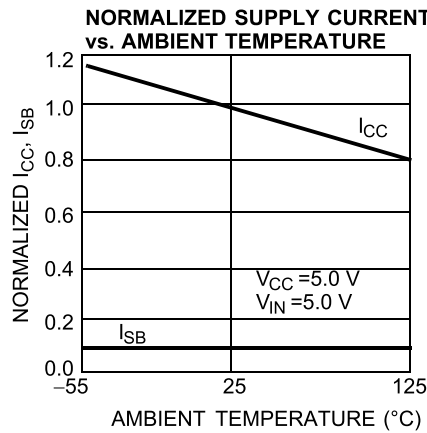
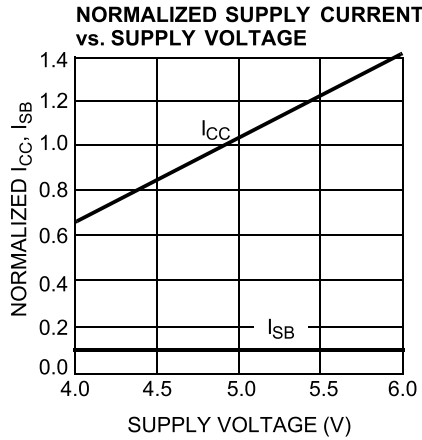
Figure 7. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [15, 16]



Notes

- 15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 16. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 17. During this period, the I/Os are in output state and input signals should not be applied.

### Typical DC and AC Characteristics



**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

**Address Designators**

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

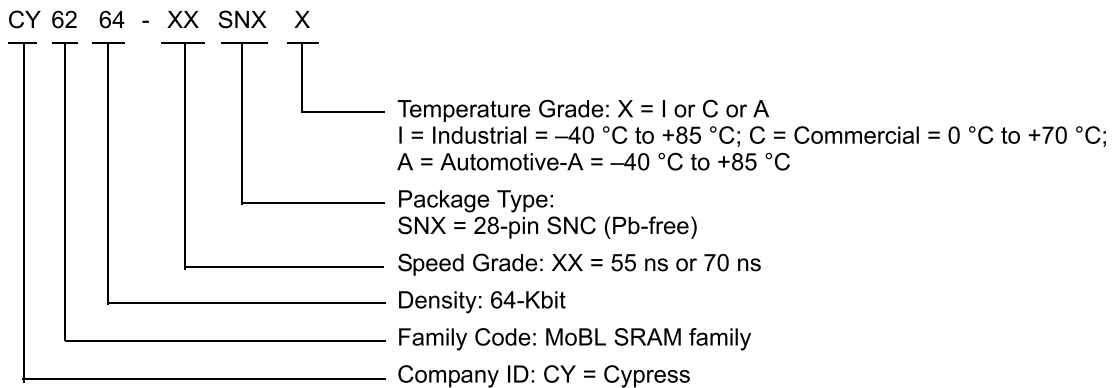
## Ordering Information

Table 1 lists the CY6264 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and see the product summary page at <http://www.cypress.com/products>.

**Table 1. Static RAM Key Features and Ordering Information**

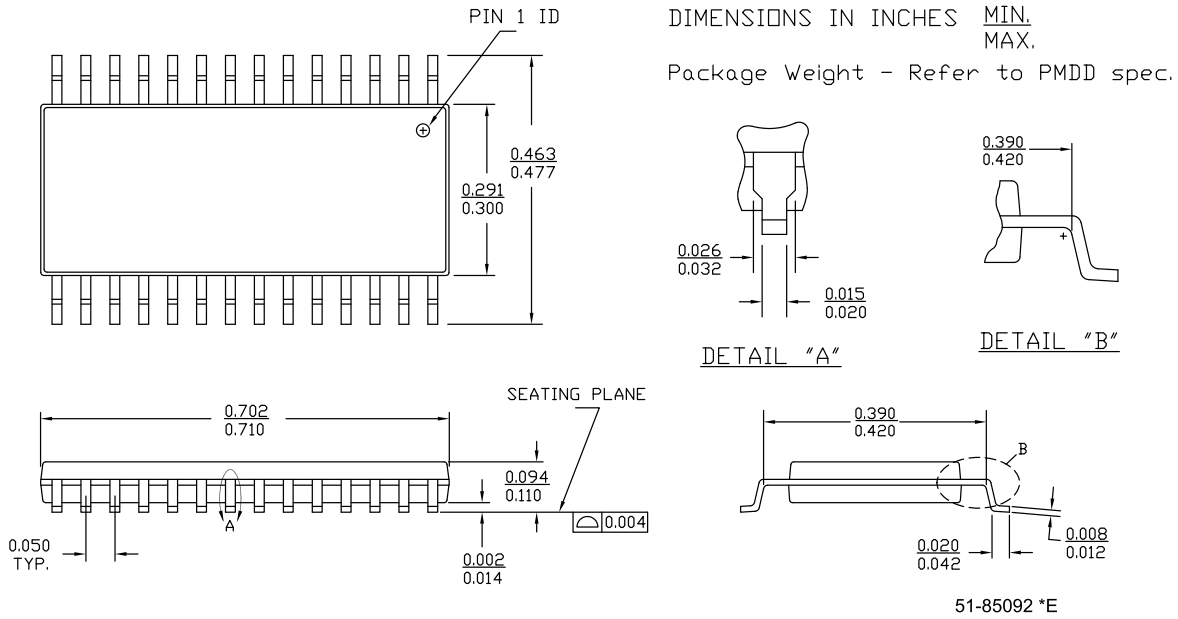
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY6264-55SNXI	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Industrial
70	CY6264-70SNXC		28-pin SNC (300 Mils) Narrow Body (Pb-free)	Commercial

## Ordering Code Definitions



**Package Diagram**

**Figure 8. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092**



## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY6264, 8 K × 8 Static RAM Document Number: 001-02367				
Revision	ECN	Orig. of Change	Submission date	Description of Change
**	384870	PCI	06/28/05	Spec # change from 38-00425 to 001-02367
*A	488954	VKN	See ECN	Added Automotive product Added 55 ns Industrial spec Removed SOIC package from the product offering Changed the description of I <sub>LX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I <sub>OS</sub> parameter from DC Electrical Characteristics table Updated ordering Information table
*B	2892510	VKN	See ECN	Updated Ordering Information table Updated Package Diagram Added Sales, Solutions, and Legal Information
*C	3329873	RAME	07/27/11	Updated template and styles according to current Cypress standards. Added acronyms, units, and ordering code definitions. Removed reference to AN1064 SRAM system guidelines.
*D	4122787	VINI	09/13/2013	Updated <a href="#">Package Diagram</a> : spec 51-85092 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.
*E	4525875	VINI	10/06/2014	Updated <a href="#">Maximum Ratings</a> : Referred Note 1 in “Supply voltage to ground potential”. Updated <a href="#">Switching Characteristics</a> : Added Note 7 and referred the same note in “WRITE CYCLE”. Updated <a href="#">Switching Waveforms</a> : Added <a href="#">Figure 7</a> . Added Note 15, 16, 17 and referred the same notes in <a href="#">Figure 7</a> . Completing Sunset Review.
*F	4576406	VINI	01/16/2015	Added related documentation hyperlink in page 1. Removed the prune part number CY6264-70SNXA in <a href="#">Ordering Information</a> .

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a>
<a href="#">Memory</a>	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

#### PSoC® Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](http://cypress.com/go/support)

---

© Cypress Semiconductor Corporation, 2005-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.